SPARCclassic Engine OEM Technical Manual

PART ONE

Sun Microsystems, Inc.
2550 Garcia Avenue
Mountain View, CA 94043
U.S.A.

Part No:. 801-3137-10
Revision A, April, 1993

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Electromagnetic Compatibility Information – U.S.A.

System Classes

Please read all of the following information to determine the class of system you have and the environment in which it should be installed and operated.

In the United States, the Federal Communications Commission (FCC) governs the levels of electromagnetic emissions from a digital device. Electromagnetic emissions can interfere with radio and television transmission. To reduce the risk of harmful interference the FCC has established requirements for manufacturers of digital devices.

A manufacturer of a digital device must test and label the product to inform an end-user of the maximum emission level from the product when used in accordance with its instructions. The FCC has established two classes of levels, Class A and Class B. A system which meets the FCC Class A requirements may be marketed for use in an industrial or a commercial area. A system which meets the more stringent FCC Class B requirements may be marketed for use in a residential area in addition to an industrial or a commercial area.

An end-user in the United States is responsible for ensuring that his system is suitable for its environment as stated in the above paragraph and bears the financial responsibility for correcting harmful interference.

For a system to be considered an FCC Class B system, all peripherals of the system (workstation, monitor, keyboard, mouse, external disk and tape drives, modem, printer, etc.) must be labeled as such. If any peripheral or the workstation itself is labeled as FCC Class A, the entire system becomes FCC Class A and should not be used in a residential area.

To determine if your system is FCC Class A or FCC Class B, you must check the marking on each peripheral and on your workstation. Each piece of equipment should have an FCC statement marked on the unit. The FCC statement should identify the equipment as Class A or Class B. If there is no indication of the Class in the FCC statement, consider it to be Class A unless there is a mark which states "FCC ID:" followed by alpha-numeric characters. If it has this FCC ID mark, it is Class B. If any of the peripherals in your system is not marked with an FCC statement, the equipment should not be used in a home because of the greater likelihood of interference to radio and television reception. Contact the manufacturer of the peripheral if you have any questions.

If an SBus board is added to the workstation by the end-user, the FCC Class of the machine could be affected. An SBus board should be marked to indicate the FCC Class of the board. If an FCC Class A SBus board is added to an FCC Class B workstation, the system becomes FCC Class A.

Modifications

If the end-user adds single inline memory modules (SIMMs) or internal drives to the workstation, the FCC Class of the machine could be affected. All SIMMs and internal drives offered by Sun for use in a Sun Workstation have been tested and will not change the FCC Class labeled on the workstation if installed per the instructions in the Sun Installation Guide.

If memory or drives are purchased from sources other than Sun, the FCC Class of the workstation may be adversely affected. Modifications not approved by Sun may void the authority granted by the FCC to operate the equipment.

Shielded Cables

Connections between the workstation and peripherals must be made using shielded cables in order to maintain compliance with FCC radio frequency emission limits.

One of the following notices applies to your system. Please reference the appropriate statement.

FCC Class A Notice

If your system is FCC Class A, the following applies:

Note – This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Class B Notice

If your system is FCC Class B, the following applies:

Note – This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Electromagnetic Compatibility Information – Canada

Communications Canada (i.e. the Department of Communications) regulates digital devices similar to the FCC in the United States. Every product should be labeled or provided with documentation which states the class of the product. The DOC defines the environment in which a digital device should be used as the FCC does, DOC Class A is for an industrial or a commercial area and DOC Class B is for a residential, an industrial, or a commercial area.

As it is with the FCC, every peripheral of a system must meet DOC Class B levels in order for a system to be considered DOC Class B. If any peripheral or the workstation is DOC Class A, the system is DOC Class A and should not be used in a residential area.

An end-user in Canada is responsible for ensuring that his system is suitable for its environment as stated in the above paragraph.

To determine if your system is DOC Class A or DOC Class B, you must check the marking on each peripheral and on your workstation. Each piece of equipment should have a DOC marking on the unit or a notice included with the equipment stating the DOC Class. If any peripheral or workstation does not have any indication of the DOC Class, consult the manufacturer of the product.

If an SBus board is added to the workstation by the end-user, the DOC Class of the machine could be affected. An SBus board should be marked to indicate the DOC Class of the board or a notice stating the DOC Class should be included. If a DOC Class A SBus board is added to a DOC Class B workstation, the system becomes DOC Class A.

If single inline memory modules (SIMMs) or internal drives are added to the workstation, the DOC Class of the machine could be affected. All SIMMs and internal drives offered by Sun for use in a Sun Workstation have been tested and will not change the DOC Class labeled on the workstation if installed per the instructions in the Sun Installation Guide. If memory or drives are purchased from sources other than Sun, the DOC Class of the workstation may be adversely affected.

One of the following notices applies to your system. Please reference the appropriate statement.

DOC Class A Notice

If your system is DOC Class A, the following applies:

This digital apparatus does not exceed Class A limits for radio noise emission for a digital apparatus as set out in the Radio Interference Regulations of the Canadian Department of Communications.

DOC Class B Notice

If your system is DOC Class B, the following applies:

This digital apparatus does not exceed Class B limits for radio noise emission for a digital apparatus as set out in the Radio Interference Regulations of the Canadian Department of Communications.

Renseignements de compatibilité électromagnetique – Canada

Communications Canada (c'est-à-dire le DOC, Ministère des Communications) règlemente les dispositifs numériques de façon analogue aux presciptions de la FCC (Commission fédérale des communications) aux Etats Unis. Chaque produit doit être étiqueté ou livré avec une documentation spécifiant sa classe. Le DOC définit, comme le fait la FCC, l'environnement dans lequel un dispositif numérique doit être utilisé. La classe A, spécifiée par le DOC, s'applique aux zones industrielles ou commerciales, alors que la classe B s'applique aux zones résidentielles, industrielles ou commerciales.

Comme il en est le cas avec la FCC, chaque périphérique d'un système doit répondre aux spécifications de la classe B définie par le DOC afin qu'un système puisse être considéré comme faisant partie de cette classe. Si un périphérique ou un poste de travail quelconque appartient à la classe A, le système appartient alors à la classe A définie par le DOC et par conséquent ne doit pas être mis en service dans une zone résidentielle.

Au Canada il revient à l'utilisateur de s'assurer que son système est approprié pour l'environnement auquel il appartient, tel que spécifié dans le paragraphe ci-dessus.

Pour déterminer si votre système appartient à la classe A ou B définie par le DOC, vous devez vérifier le marquage figurant sur chaque périphérique ainsi que sur votre poste de travail. Toute pièce de matériel doit porter un marquage du DOC ou être accompagnée d'un document spécifiant la classe DOC à laquelle elle appartient. Si aucune référence à la classe définie par le DOC n'est présente sur un périphérique ou un poste de travail, contactez le fabricant du produit.

Si l'utilisateur ajoute une carte de type SBus au poste de travail, cela risque d'affecter la classe définie par le DOC. Une carte de type SBus doit être marquée pour indiquer à quelle classe elle appartient, ou un document spécifiant sa classe doit l'accompagner. Si une carte de type SBus de la classe A du DOC est ajoutée à un poste de travail de la classe B, le système appartiendra alors à la classe A, telle qu'elle est définie par le DOC.

Si des unités internes ou des barrettes de mémoire SIMM sont ajoutées à un poste de travail, la classe du DOC de la machine risque d'être affectée. Toutes les unités internes et barrettes de mémoire SIMM offertes par Sun et destinées à être utilisées sur un poste de travail Sun ont été soumises à des essais. Elles ne changeront pas la classe du DOC figurant sur le poste de travail si l'installation est conformée aux instructions spécifiées dans le Guide d'installation Sun. Si l'utilisateur se procure des unités et des barrettes de mémoire ailleurs que chez Sun, la classe du poste de travail définie par le DOC risque d'être défavorablement affectée.

Veuillez consulter celui des avis suivants qui s'applique à votre système:

Avis concernant les systèmes appartenant à la classe A du DOC:

Si votre système appartient à la classe A du DOC, ce qui suit s'y applique:

Le présent appareil numérique n'émet pas de bruits radioélectriques dépassant les limites applicables aux appareils numériques de la classe A prescrites dans le Règlement sur le brouillage radioélectrique édicté par le Ministère des Communications du Canada.

Avis concernant les systèmes appartenant à la classe B du DOC:

Si votre système appartient à la classe B du DOC, ce qui suit s'y applique:

Le présent appareil numérique n'émet pas de bruits radioélectriques dépassant les limites applicables aux appareils numériques de la classe B prescrites dans le Règlement sur le brouillage radioélectrique édicté par le Ministère des Communications du Canada.

Informationen zur Elektromagnetischen Kompatibilität — Bundesrepublik Deutschland (Federal Republic of Germany)

Hiermit wird bescheinigt, dass die Desktop SPARCstation in Übereinstimmung mit den Bestimmungen der Verfügung 243/1991 funkenstört ist. Der Deutschen Bundespost wurde das inverkehrbringen dieses Gerätes angezeigt und die Berechtigung zur Überprüfung der Serie auf Einhaltung der Bestimmungen eingeräumt.

Sun Microsystems, Incorporated: 2550 Garcia Avenue, Mountain View, California, 94043-1100 U.S.A.

Safety Agency Compliance

The following text provides safety precautions to follow when installing a Sun Microsystems, Inc., product.

Safety Precautions

For your protection, observe the following safety precautions when setting up your equipment:

- Follow all warnings and instructions marked on the equipment.
- Ensure that the voltage and frequency of your power source matches the voltage and frequency inscribed on the equipment's electrical rating label.
- Never push objects of any kind through openings in the equipment. Dangerous voltages may be present. Conductive foreign objects could produce a short circuit that could cause fire, electric shock, or damage to your equipment.

Symbols

The following symbols appear in this book.

Caution – There is risk of personal injury and equipment damage. Follow the instructions.

Warning – Hazardous voltages are present. To reduce the risk of electric shock and danger to personal health, follow the instructions.

On: The principal on/off switch is in the On position.

Off: The principal on/off switch is in the Off position.

Standby: The principal on/standby switch is in the standby position. AC voltage is still present within the power supply.

Modifications to Equipment

Do not make mechanical or electrical modifications to the equipment. Sun Microsystems, Inc., is not responsible for regulatory compliance of a modified Sun product.

Placement of a Sun Product

Caution – To ensure reliable operation of your Sun product and to protect it from overheating, openings in the equipment must not be blocked or covered. A Sun product should never be placed near a radiator or heat register.

Power Cord Connection

Warning – Sun products are designed to work with single-phase power systems having a grounded neutral conductor. To reduce the risk of electrical shock, do not plug Sun products into any other type of power system. Contact your facilities manager or a qualified electrician if you are not sure what type of power is supplied to your building.

Warning – Not all power cords have the same current ratings. Household extension cords do not have overload protection and are not meant for use with computer systems. Do not use household extension cords with your Sun product.

Lithium Battery

Caution – On Sun CPU boards, there is a lithium battery molded into the real-time clock, SGS No. MK48T08. Batteries are not customer replaceable parts. They may explode if mistreated. Do not dispose of the battery in fire. Do not disassemble it or attempt to recharge it.

Caution – It is not safe to operate Sun products without the top cover in place. Failure to take this precaution may result in personal injury and system damage.

SELV Compliance

Safety status of I/O connections comply to SELV requirements.

Conformité aux normes de sécurité

Cette texte traite des mesures de sécurité qu'il convient de suivre pour l'installation d'un produit Sun Microsystems, Inc.

Mesures de sécurité

Pour votre protection, veuillez prendre les précautions suivantes pendant l'installation du matériel:

- Suivre tous les avertissements et toutes les instructions inscrites sur le matériel.
- Vérifier que la tension et la fréquence de la source d'alimentation électrique correspondent à la tension et à la fréquence indiquées sur l'étiquette de classification de l'appareil.
- Ne jamais introduire d'objet quel qu'il soit dans une des ouvertures de l'appareil. Vous pourriez vous trouver en présence d'éléments haute tension. Tout objet conducteur introduit de la sorte pourrait produire un court-circuit qui entraînerait des flammes, des risques d'électrocution ou des dégâts matériels.

Symboles

Vous trouverez ci-dessous la signification des différents symboles utilisés:

Attention : Risques de blessures corporelles et de dégâts matériels. Veuillez suivre les instructions.

Danger : Présence de tensions dangereuses. Pour éviter les risques d'électrocution et de danger pour la santé physique, veuillez suivre les instructions.

Marche : Le commutateur marche/arrêt principal est en position de *marche.*

Arrêt : Le commutateur marche/arrêt principal est en position *d'arrêt.*

Veille : L'interrupteur principal MARCHE/VEILLE est en position VEILLE. Attention, la tension secteur reste presente.

Modification *du matériel*

Ne pas apporter de modification mécanique ou électrique au matériel. Sun Microsystems, Inc., n'est pas responsable de la conformité réglementaire d'un produit Sun qui a été modifié.

Positionnement d'un produit Sun

Attention : Pour assurer le bon fonctionnement de votre produit Sun et pour l'empêcher de surchauffer, il convient de ne pas obstruer ni recouvrir les ouvertures prévues dans l'appareil. Un produit Sun ne doit jamais être placé à proximité d'un radiateur ou d'un registre de chaleur.

Connexion du cordon d'alimentation

Danger : Les produits Sun sont conçus pour fonctionner avec des alimentations monophasées munies d'un conducteur neutre mis à la terre. Pour écarter les risques d'électrocution, ne pas brancher de produit Sun dans un autre type d'alimentation secteur. En cas de doute quant au type d'alimentation électrique du local, veuillez vous adresser au directeur de l'exploitation ou à un électricien qualifié.

Danger : Tous les cordons d'alimentation n'ont pas forcément la même puissance nominale en matière de courant. Les rallonges d'usage domestique n'offrent pas de protection contre les surcharges et ne sont pas prévues pour les systèmes d'ordinateurs. Ne pas utiliser de rallonge d'usage domestique avec votre produit Sun.

Batterie au lithium

Attention : Sur les cartes UC Sun, une batterie au lithium (référence MK48T08) a été moulée dans l'horloge temps réel SGS. Les batteries *ne sont pas* des pièces remplaçables par le client. Elles risquent d'exploser en cas de mauvais traitement. Ne pas jeter la batterie au feu. Ne pas la démonter ni tenter de la recharger.

Attention : Il est dangereux de faire fonctionner un produit Sun sans le couvercle en place. Si l'on néglige cette précaution, on encourt des risques de blessures corporelles et de dégâts matériels.

SELV conformité

Sécurité : les raccordements E/S sont conformes aux normes SELV.

Sicherheitsbehördliche Vorschriften

In diesem Vorwort werden die Sicherheitsmaßnahmen beschrieben, die bei der Installation eines Produkts von Sun Microsystems, Inc., zu befolgen sind.

Sicherheits-maßnahmen

Beachten Sie zu Ihrem eigenen Schutz die folgenden Sicherheitsmaßnahmen, wenn Sie Ihre Geräte aufbauen:

- Beachten Sie alle auf den Geräten angebrachten Warnungen und Anweisungen.
- Vergewissern Sie sich, daß Spannung und Frequenz Ihrer Stromquelle mit der Spannung und Frequenz übereinstimmen, die auf dem Etikett mit den elektrischen Nennwerten des Geräts angegeben sind.
- Stecken Sie niemals irgendwelche Gegenstände in Öffnungen in den Geräten. Es Sie können gefährliche Spannungen vorliegen. Leitfähige fremde Gegenstände könnten einen Kurzschluß verursachen, der zu Feuer, Elektroschock oder einer Beschädigung Ihrer Geräte führen könnte.

Symbole

Die verwendeten Symbole haben die folgende Bedeutung:

Vorsicht – Gefahr von Personenverletzung und Geräteschäden. Anweisungen befolgen.

Warnung – Gefährliche Spannungen. Zur Reduzierung des Elektroschockrisikos und der Gesundheitsgefährdung die Anweisungen befolgen.

Ein: Der Hauptschalter steht auf *Ein*.

Aus: Der Hauptschalter steht auf *Aus*.

Standby: Der Hauptschalter ON/STANDBY steht auf STANDBY. Das Gerät ist in Wartestellung.

Änderung der Geräte

Nehmen Sie keine mechanischen oder elektrischen Änderungen an den Geräten vor. Sun Microsystems, Inc., ist nicht verantwortlich für die Einhaltung behördlicher Vorschriften, wenn an einem Sun-Produkt Änderungen vorgenommen wurden.

Aufstellungsort eines Sun-Produkts

Vorsicht – Um einen zuverlässigen Betrieb Ihres Sun-Produkts zu gewährleisten und es vor Überhitzung zu schützen, dürfen die Öffnungen im Gerät nicht blockiert oder bedeckt werden. Ein Sun-Produkt sollte niemals in der Nähe eines Heizkörpers oder einer Heizluftklappe aufgestellt werden.

Anschluß des Stromkabels

Warnung – Sun-Produkte sind für den Betrieb mit Einphasen-Stromsystemen mit einem geerdeten Mittelleiter vorgesehen. Um die Elektroschockgefahr zu reduzieren, schließen Sie Sun-Produkte nicht an andere Arten von Stromsystemen an. Wenden Sie sich an Ihren Anlagenleiter oder einen qualifizierten Elektriker, wenn Sie sich nicht sicher sind, welche Art von Strom Ihr Gebäude erhält.

Warnung – Nicht alle Stromkabel besitzen die gleichen Stromnennwerte. Haushaltsverlängerungsschnuren haben keinen Überlastungsschutz und sind nicht zum Gebrauch mit Computersystemen bestimmt. Benutzen Sie keine Haushaltsverlängerungsschnuren für Ihr Sun-Produkt.

Lithiumbatterie

Vorsicht – Eine Lithiumbatterie ist in die SGS-Echtzeituhr, Nr. MK48T08, von Sun-CPU-Karten eingepreßt. Batterien können *nicht* vom Kunden ausgewechselt werden. Bei falscher Behandlung können sie explodieren. Batterien nicht in Feuer werfen und nicht auseinandernehmen oder wiederaufladen.

Vorsicht – Der Betrieb von Sun-Produkten ohne obere Abdeckung ist nicht sicher. Bei Nichteinhalten dieser Vorsichtsmaßregel kann es zu Personenverletzung und Systemschäden kommen.

SELV Vorschriften

Die E/A-Anschlüsse erfüllen die Sicherheitsanforderungen der SELV-Norm.

Conformidad con la agencia de seguridad

Este prólogo presenta las precauciones de seguridad a seguir cuando se instala un producto de Sun Microsystems, Inc.

Precauciones de seguridad

Para su protección, observe las siguientes precauciones de seguridad al instalar su equipo:

- Siga todos los avisos e instrucciones marcados en el equipo.
- Asegúrese de que el voltaje y la frecuencia de su fuente de alimentación sean iguales al voltaje y frecuencia indicados en la etiqueta de la capacidad eléctrica nominal del equipo.
- No introduzca jamás objetos de ninguna clase por las aberturas del equipo porque pueden estar presentes voltajes peligrosos. Cualquier objeto conductor extraño puede producir cortocircuito que podría causar incendio, electrochoque, o daños a su equipo.

Símbolos

Los siguientes símbolos significan:

Precaución – Peligro de lesión personal y daño al equipo. Siga las instrucciones.

Aviso – Hay presentes voltajes peligrosos. Siga las instrucciones para reducir el riesgo de electrochoque y los peligros contra la salud.

Encendido (On): El interruptor principal de encendido/apagado está en la posición de *encendido*.

Apagado (Off): El interruptor principal de encendido/apagado está en la posición de *apagado*.

Espera: El interruptor principal de encendido/espera se encuentra en la posición de espera. El suministro de energía eléctrica continúa recibiendo tensión de corriente alterna.

Modificaciones al equipo

No haga modificaciones mecánicas o eléctricas al equipo. Sun Microsystems, Inc., no se hace responsable del cumplimiento de las regulaciones de un producto Sun si ha sido modificado.

Colocación de un producto Sun

Precaución – Para lograr un funcionamiento seguro de su producto Sun y para protegerlo contra el calentamiento excesivo, no se deben bloquear o cubrir las aberturas del aparato. Ningún producto Sun se debe colocar jamás cerca de un radiador o una fuente térmica.

Conexión del cable de alimentación

Aviso – Los productos Sun han sido diseñados para funcionar con sistemas de alimentación monofásicos que tengan un conductor neutro a tierra. Para reducir el riesgo de electrochoque, no enchufe los productos Sun a ningún otro tipo de sistema de alimentación. Si no está seguro del tipo de alimentación eléctrica que se suministra a su edificio, consulte al administrador de la propiedad o a un electricista profesional.

Aviso – No todos los cables de alimentación tienen la misma capacidad nominal de corriente. Las extensiones tipo caseras no tienen protección contra sobrecargas y no están destinadas a usarse con sistemas de computación. No use extensiones caseras con su producto Sun.

Batería de litio

Precaución – En los tableros de la CPU de Sun, viene instalada una batería de litio moldeada a reloj de tiempo real, SGS No. MK48T08. El cliente *no* debe cambiar las baterías porque pueden estallar si no se manejan como es debido. No se deshaga de las baterías echándolas al fuego. No las desmonte ni trate de volverlas a cargar.

Precaución – Los productos Sun no pueden funcionar sin riesgo si la cubierta superior no está colocada en su sitio. Si no toma esta precaución, correrá el riesgo de lesionarse personalmente y dañar el equipo.

SELV conformidad

La seguridad de las conecciónes de entrada-salida cumplen con las normas de seguridad para baja tensión (SELV).

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Preface

This preliminary SPARCclassic Engine OEM Technical Manual is a description of the SPARCclassic Engine board, its connectors, ASICs, ports, and functional description, along with a programmer's model.

An optional SPARCclassic Engine I/O board (with workstation I/O connectors) is defined in the appendices.

Using This Guide

The ***SPARCclassic Engine OEM Technical Manual*** contains hardware and firmware information about the Sun Microsystems SPARCengine™ EC (Embedded Controller) board product.

This preface provides information that helps you use the ***SPARCclassic Engine OEM Technical Manual,*** including the following topics:

- audience definition
- thumbnail sketch of the contents
- font usage definitions
- textual conventions
- support documentation
- instructions on where to get Sun help for the SPARCclassic Engine hardware/software

Audience

The ***SPARCclassic Engine OEM Technical Manual*** is written for computer hardware engineers, system programmers, computer technicians, and others involved in setting up prototype hardware using the SPARCclassic Engine board.

All readers should have an understanding of electronic hardware, operating system software interfacing with hardware, communication (bus) standards, and related computer concepts.

How to Read the Guide

Read through this document once, sequentially. Use this guide as a reference document thereafter.

A considerable amount of the technical information about SPARCclassic Engine exists in other documents. Some additional documents are gathered in the appendices. Other documents are only referenced.

Organization of the OEM Technical Manual

The organization of the ***SPARCclassic Engine OEM Technical Manual*** is divided into four major sections and an appendix, as listed on the next page.

Sections of OEM Technical Manual	Chapter Numbers	Chapter Titles
Introducing SPARCclassic Engine	Chapter 1	Using This Guide
	Chapter 2	Safety Considerations
	Chapter 3	Quick Reference Guide
	Chapter 4	Features
	Chapter 5	Specifications
	Chapter 6	Functional Overview
Hardware Interface	Chapter 7	Removal and Replacement Procedures
Software Interface	Chapter 8	Programmer's Guide
	Chapter 9	Open Boot PROM
	Chapter 10	Diagnostics
Appendices	Appendix A	SPARCclassic Engine Mechanical Drawings
	Appendix B	SPARCclassic Engine Schematics
	Appendix C	SPARCclassic Engine Pinouts
	Appendix D	4 MB DRAM Specifications
	Appendix E	16 MB DRAM Specifications
	Appendix F	160-Pin Connector Specifications
	Appendix G	I/O Board Specifications
	Appendix H	I/O Board Mechanical Drawings
	Appendix I	I/O Board Schematics
	Appendix J	I/O Board Pinouts
	Appendix K	TI microSPARC Reference Manual
	Appendix L	TI microSPARC Data Sheet
	Appendix M	NCR SBus I/O Chipset Specifications
Revision History		

Textual Conventions

Abbreviations

Memory size measurements are displayed with the following abbreviations:

bit	binary digit (one bit)
Kbits	Kilobits (one thousand bits)
Mbits	Megabits (one million bits)
byte	one group of eight bits
KB	Kilobytes (one thousand bytes)
MB	Megabytes (one million bytes)
GB	Gigabytes (one billion bytes)

Performance measurements are displayed with the following abbreviations:

MFLOPS	Millions of Floating-Point Operations per second
MIPS	Million Instructions per second
Mbps	Million bits per second

Time measurement is displayed with the following abbreviation:

nsec	nano-seconds

Addressing Nomenclature

An "0x" before a number indicates that the number is hexadecimal. For example, 0x0000 000F indicates a hexadecimal value of "16."

Full 32-bit address locations are indicated by the hexadecimal values displayed with a space between the fourth and fifth digit for easy readability:

0x6000 0000

Throughout the guide, addresses are provided in the following fashion:

PA 0x6000 0000
VA 0x6000 0000

The PA stands for physical address, and VA stands for virtual address.

Where it is necessary to show that an address has a range, it may be shown with the variable part shown as an x.

VA 0x2000 xxxx

This is translated as the entire space between VA 0x2000 0000 and VA 0x2000 FFFF (inclusive).

Address bits are shown as follows:

PA[31:24]

This is translated into text as "physical address bits 31 through 24."

Data bits are shown as follows:

D[31:24]

This is translated into text as "data bits 31 through 24."

Font Conventions

Palatino Font

The primary text/header font used in this guide is Palatino.

- body text
- chapter names
- titles of reference documentation
- variables when describing a software command syntax

Courier Font

Courier is used to indicate screen text of the Sun Workstation.

- screen text described within body text including path names and file names
- screen text within a screen box
- user input

Where to Get Help

Hardware Support

Sun Microsystems, under contract with your company, performs all hardware support, including replacing malfunctioning boards. Send all non-functioning boards to the address listed in the support contract.

Software Support

Contact Sun Consulting for all support questions on SPARCclassic Engine software.

Safety Considerations

Safety Precautions

There are few safety concerns about the SeEC itself. The board has only one part that can cause you harm, a lithium battery for the NVRAM/TOD. The battery would only be a problem when it is severely mistreated.

However, the power supply and various other components that you might use to create a 'system,' even for test, call for careful handling. This manual cannot predict what components you may use in creating a working system, and therefore, cannot provide specific warnings about such components.

Be sure to read carefully the safety documentation supplied with the components that you use with the SeEC.

The following international symbols appear in this book when you must perform procedures requiring proximity to electrical current.

Caution - There is risk of personal injury and equipment damage. Follow the instructions.

Warning - Hazardous voltages are present. To reduce the risk of electric shock and danger to personal health, follow the instructions.

Safety information is contained in a section titled "Safety Agency Compliance" in the front of this book. Be sure to read the entire section before installing and operating this equipment. This information also appears after the English version in French, German, and Spanish translations.

Sample Caution Statement

Caution statements throughout the manual look like the following sample:

Caution – Be careful of electrostatic discharge (ESD) with the SeEC board. Use appropriate ESD reduction procedures.

Sample Warning Statement

Warning statements throughout the manual look like the following sample:

Warning – Verify that the system power switch is in the Standby (⏻) position. The green LED at the front of the system unit should not be lit and the fan should not be running.

SPARCclassic Engine Features

The SPARCclassic Engine board is a Scalable Processor Architecture Reduced instruction set Computer (SPARC)-based computer on a single board with two SBus slots, frame-buffer, floppy disk connector, SCSI connector, JTAG testability for the major ASICs, and a single 160 pin I/O edge connector. The 160-pin edge connector is intended to mate with the SPARCclassic Engine I/O board which has a full set of workstation I/O connectors.

3.1 SPARCclassic Engine

- SPARCclassic Engine performance (see **Chapter 4** for testing configuration):
  - CPU: 59.1 MIPS (Dhrystone V1.1) @ 50 MHz performance
  - FPU: 4.6 MFLOPS (Linpack Double-performance) @ 50 MHz performance
- Sun-custom low-power CMOS integrated ASICs for high reliability:
  - One microSPARC (SPARC Version 8 compatible RISC microprocessor)
    - SPARC IU
    - SPARC FPU
    - Cache controller
    - Instruction cache (4 KB)
    - Data cache (2 KB)
    - SPARC Reference MMU
    - I/O MMU
    - RAM controller (main memory)
    - SBus controller
    - JTAG internal/boundary scan controller
  - One NCR89C100 (master I/O controller)

- DMA2 controller
- SCSI (ESP) controller
- Ethernet (LANCE-compatible) controller
- Parallel (printer) (Centronics) controller
- JTAG internal/boundary scan controller

- One NCR89C105 (slave I/O controller)
  - Serial A controller (full duplex)
  - Serial B controller (full duplex)
  - Floppy disk drive controller
  - Interrupt controller
  - Reset controller
  - Power on/off controller
  - Counter/timer controls
  - EPROM/NVRAM controller
  - JTAG internal/boundary scan controller

- Other ASICs:
  - One video controller (video controller) (virtual SBus CG3 card)
    - On-board video controller (S-4 Video)
    - 1152 x 900 resolution
    - 1024 x 768 SVGA resolution
    - 8-bits per pixel (color & grayscale)
    - 1-bit per pixel (monochrome)
    - 256 colors from palette of over 16 million colors
    - Color RAMDAC (Bt458)
    - No VRAM SIMM slot
  - One audio controller 8-bit sound
  - Eight 128K x 8 VRAM chips (1 MB VRAM soldered on-board)
  - One monolithic triple 8-bit RAMDAC
  - One 256 KB boot PROM (EPROM)
  - One 8 KB TOD/NVRAM (with battery backup)
  - 1 MB VRAM soldered on-board
- Connectors
  - Six female DRAM SIMM 160-pin connectors
    - supports 4 and 16 MB SIMMs
    - up to 96 MB of on-board main memory expansion (16 MB SIMMS)
    - one parity bit per 32-bit word
    - 64-bit memory bus
  - Two female SBus master/slave connectors (25 MHz)
    - 32-bit data path
    - 32-bit virtual address for master, 28-bit physical address per slave

- Maximum 16 byte burst
- One female SCSI 50-pin ribbon-type connector
- One female floppy 34-pin ribbon-type connector
- One male board power 26-pin edge connector
- One male I/O 160-pin edge connector
  - all signals for I/O board connectors
  - all signals for CPU board connectors (SBus not included)
  - JTAG signals for major ASICs

3.2 *SPARCclassic Engine Supported Standards*

- Fully compatible with SunOS 5.1 and Solaris 2.1 (or higher)
  - Binary compatible with SPARCware applications (Solaris 1.0 or later)
- Hardware standards compliant:
  - SPARC International SPARC Architecture 8.0
- Software standards compliant:
  - SPARC International SPARC Compliance Definition 2.0
  - IEEE POSIX standard 1003.1 (1988)
  - X/Open-XPG3 component branded
  - XPG2 BASE branded
  - System V Interface Definition Issue II
- Supports standards in application software:
  - SPARC standards
  - OpenLook standards
  - Sun UNIX standards
- 3000+ SPARCware applications

SPARCclassic Engine Specifications

4.1 SPARCclassic Engine Hardware Specifications

Category	Specifications
Physical Dimensions	
CPU Board Size:	
Long axis	228.96 mm (9.00 in.)
Short axis	226.09 mm (8.89 in.)
Edge to Trace Distance	0.50 mm (0.10 in.) nearest to edge
Edge to Component	0.00 mm (0.00 inches) opposite from 160-pin conn.
Microprocessor Performance Figures	
Measurement Configuration:	Hardware: 50 MHz microSPARC, 48 MB of RAM Software: Solaris 2.1 Beta 2.0 SPARC C 3.0 alpha, KAP (SPECint92) Apogee 0.82 alpha, KAP (SPECfp92, Dhrystone. Linpack)
IU Performance	59.1 MIPS (Dhrystone V1.1)
FPU Performance	4.6 MFLOPS (Linpack 1000 Double Precision)
SPECint92	26.4
SPECfp92	21.0

Category	Specifications
RISC Microprocessor	
Microprocessor	1 microSPARC
IU	SPARC IU
FPU	Meiko Design FPU
Cache Controller	Cache
Memory Controller	SPARC Reference MMU
Testing Support	JTAG scan support, built-in self-testing
Packaging	288-pin 10-mil pitch TAB
Integer Unit	Sun Microsystems SPARC IU
IU Performance	59.1 MIPS @ 50 MHz
Architecture	Harvard
Cache Streaming Support	Instruction and Data
Floating Point Unit	Meiko Design FPU
FPU Performance	4.6 MFLOPS @ 50 MHz
Instructions	Single and double precision
Cache Instruction	4 KB direct-mapped write-through, virtual indexed, physical tagged
Cache Data	2 KB direct-mapped write-through virtual indexed, physical tagged
Cache Write Buffering	One double-word
Cache Recovery	Complete write-fault recovery supported
Cache Linesize	Instruction Cache is 32 B linesize Data Cache is 16 B linesize
Input/Output	
SBus Devices	5 master/slave devices
SBus Slots	2 physical slots
SBus Standard	SBus specifications, Revision A.2
SBus Data Size	32-bit full master/slave (all slots)
SBus Clock Rate	25 MHz (1/2 CPU Clock, 1,2,4,8,16 Bytes))
SBus Write Sizes	Maximum 16 byte burst
SBus Writes	Quad/doubleword burst mode supported

Category	Specifications
SCSI Port	1 50-pin connector and signals to 160-pin I/O connector
SCSI Standard	ANSI X3.133
SCSI Types	synchronous/asynchronous (host)
SCSI Performance	Up to 10 MB per second (synchronous) (fast)
Ethernet Port	Signals to 160-pin I/O connector: Twisted-pair signals AUI signals
Ethernet Port	1 channel TPE (RJ45) or AUI (with adaptor)
Ethernet Standard	IEEE 802.3
Parallel Port	Signals to 160-pin I/O connector
Parallel Port Standards	8-bit Centronics-compatible
Serial A/B Ports	Signals to 160-pin I/O connector
Serial Standard	RS232C
Serial Types	synchronous/asynchronous
Serial Configuration	DTE
Serial Performance	76 Kbps (hardware) 38.4 Kbps (Solaris 2.1)
K/M Port	Signals to 160-pin I/O connector
K/M Type	asynchronous
K/M Performance	19200 (19.2 Kbit) baud (maximum possible)
Floppy Disk Drive Ports	34-pin ribbon connector / 160-pin I/O connector
Audio Speaker Port	Signals to 160-pin I/O connector / 4-pin on-board
Audio Microphone Port	Signals to 160-pin I/O connector
Audio Performance	Voice standard (8-bit monophonic)
Audio Controller Chip	Am79C30A Digital Subscriber Controller (DSC)
Video Port	Signals to 160-pin I/O connector
Video Standard	Sun Microsystems
Video Controller Chip	Sun Microsystems S4-Video (CG3) compatible
Video Frequencies	Selectable within the NVRAM
JTAG Port	Signals to 160-pin I/O connector

Category	Specifications
Monitor Port	2 4-pin on-board connectors and signals to the 160-pin I/O connector
Power On/Off Port	1 3-pin on-board connector and signals to the 160-pin I/O connector
On-board Main Memory	
Type of memory	DRAM parity memory (1 parity bit per 32 bits)
On-card DRAM Banks	3
SIMMs per Bank	2
DRAM SIMM Specs	72-pin (x 33 or x 36)
DRAM Speed	60 nsec fast-page mode
DRAM Expansion Range	8 MB to 96 MB (16 MB minimum for Solaris)
On-board Video Memory	
Type of memory	VRAM, no parity
Base Memory	1 MB of VRAM (soldered to board)
On-card VRAM Banks	1 MB VRAM SIMM 160-pin connector
VRAM SIMM Specs	160-pin (x 33 or x 36)
VRAM Speed	80 nsec fast-page mode
VRAM Expansion	2 MB (combined with the 1 MB on-board)
SBus	
SBus Controller Chip	microSPARC
SBus Physical Ports	2 female SBus 160-pin connectors
Power Connectors	
Board power	2 (one 26-pin edge and one 12-pin connector)

4.2 *SPARCclassic Engine Electrical Specifications*

Power Requirements For This Product

+5VDC 0-5%
maximum 7 Amperes
(no SBus card, no hard disk drive, and no optional memory)

RS232/Ethernet Power Supply
+12VDC +8%/-10%
-12VDC +/-10%
maximum 0.0 — 0.1 Amperes
(no hard disk drive)

Power Dissipation

For a system with 40 MB of DRAM and no SBus cards:

Power Dissipation	< 33 Watts (not including SBus cards)
Typical	24 Watts
Maximum	33 Watts

SPARCclassic Workstation Power Supply Specification

AC voltage	90-132 VAC or 180-264 VAC
AC frequency	47-63 Hz
Power	200 watts (= .2 KVA)

4.3 *SPARCclassic Engine Testing Specifications*

Below, the standards supported by SPARCclassic Engine, when the board is placed in a properly-designed Faraday cage and system enclosure:

Product Testing Standards Supported by This Product	
SCD	SPARC Compliance Definition, Version 2.0
UL1950	Underwriters Laboratory (testing in U.S.A)
CSA 950-M89	Canadian Standards Association (testing in Canada)
EN 50950	Technischer Überwachungs-Verien (TUV) (testing in Europe)
CISPR 22	Class B European CENELEC EMI/RFI (testing in Europe)

Electromagnetic Compatibility Standards Supported by This Product	
FCC part 15, sub. B	Federal Communications Commission (U.S.A regulatory agency for EMI regulation)
VCCI Class 2	Voluntary Council for the Control of Interference (Japanese association for voluntary EMI regulation)
vfg 243/1991	Verband Deutscher Elektrotechniker (VDE) (German standard for EMI regulation)

4.4 *SPARCclassic Engine Environmental Specifications*

Below, the environmental specifications for the SPARCclassic Engine board are presented. NOTE: The testing was performed using a standard Sun Microsystems workstation enclosure.

Operating Environmental Requirements For This Product		
Values	**Minimum**	**Maximum**
Temperature Range	32° F (0° C)	136° F (55° C)
Humidity Range relative non-condensing at 104° F (40° C):		
	5%	95%
Wet Bulb Maximum	N/A	77° F (25° C)
Altitude Range	0 ft (0 m)	10,000 ft (3,408 m)
Vibration	5-22 Hz, 0.01 in. p-p	22-500 Hz, 0.25 in. p-p
Shock	N/A	5 g pk, 10 msec 1/2 sine wave
Non-Operating Environmental Requirements For This Product		
Temperature Range	-4° F (-20° C)	167° F (75° C)
Humidity Range relative non-condensing at 104° F (40° C):		
	5%	95%
Wet Bulb Maximum	N/A	115° F (46° C)
Altitude Range	0 ft (0 m)	40,000 ft (12,192 m)
Vibration	5-22 Hz, 0.01 in. p-p	22-500 Hz, 0.25 in. p-p
Shock	N/A	20 g pk, 30 msec

Functional Overview

5.1 SPARCclassic Engine Functional Overview

The SPARCclassic Engine is a Reduced Instruction Set Computer (RISC) chip set main logic board. Sun Microsystems' implementation of RISC on the SPARCclassic Engine is named the Scalable Processor Architecture Reduced-instruction-set Computer (SPARC).

The significant hardware units of the SPARCclassic Engine are the chips, power connector, I/O cable connectors, jumpers, I/O 160-pin board connector, DRAM connectors, and socket connectors.

5.1.1 ASICs

The chips include a microSPARC microprocessor, a master I/O (89C100) controller, a slave I/O (89C105) controller, video controller, RAMDAC controller, audio controller, NVRAM, Boot PROM. Off-board, various flavors of required/optional DRAM (main memory) and VRAM are required/optional.

5.1.2 Power Connectors

The board power connector is the only power cable connector on the SPARCclassic Engine.

5.1.3 I/O Connectors

The on-board I/O connectors include two physical SBus slots, a SCSI header, a floppy disk connector, and a monophonic speaker and LED connector.

5.1.4 160-Pin I/O Connector

In addition, all the above I/O signals (minus the SBus signals) are brought out to the 160-pin I/O edge connector, with the additional signals necessary to complete the I/O for a full workstation including SCSI, Ethernet, headphone and microphone, two serial ports, parallel port, keyboard/mouse port, and video port.

NOTE: A SPARCclassic I/O board contains all the external I/O connectors for a workstation, including SCSI, Ethernet (AUI and twisted-pair), audio (including headphone, and microphone), serial, parallel (printer), keyboard/mouse, and video (with monitor bus). See Appendix F for a full description of the SPARCclassic I/O board.

5.1.5 DRAM Connectors

Six connectors are provided for special Sun Microsystems DRAM SIMMs.

5.1.6 Socket Connectors

Two socket connectors are provided, one for the NVRAM and one for the 2 MBit (256K) EEPROM.

Figure 5-1 General Layout of the SPARCclassic Engine Board

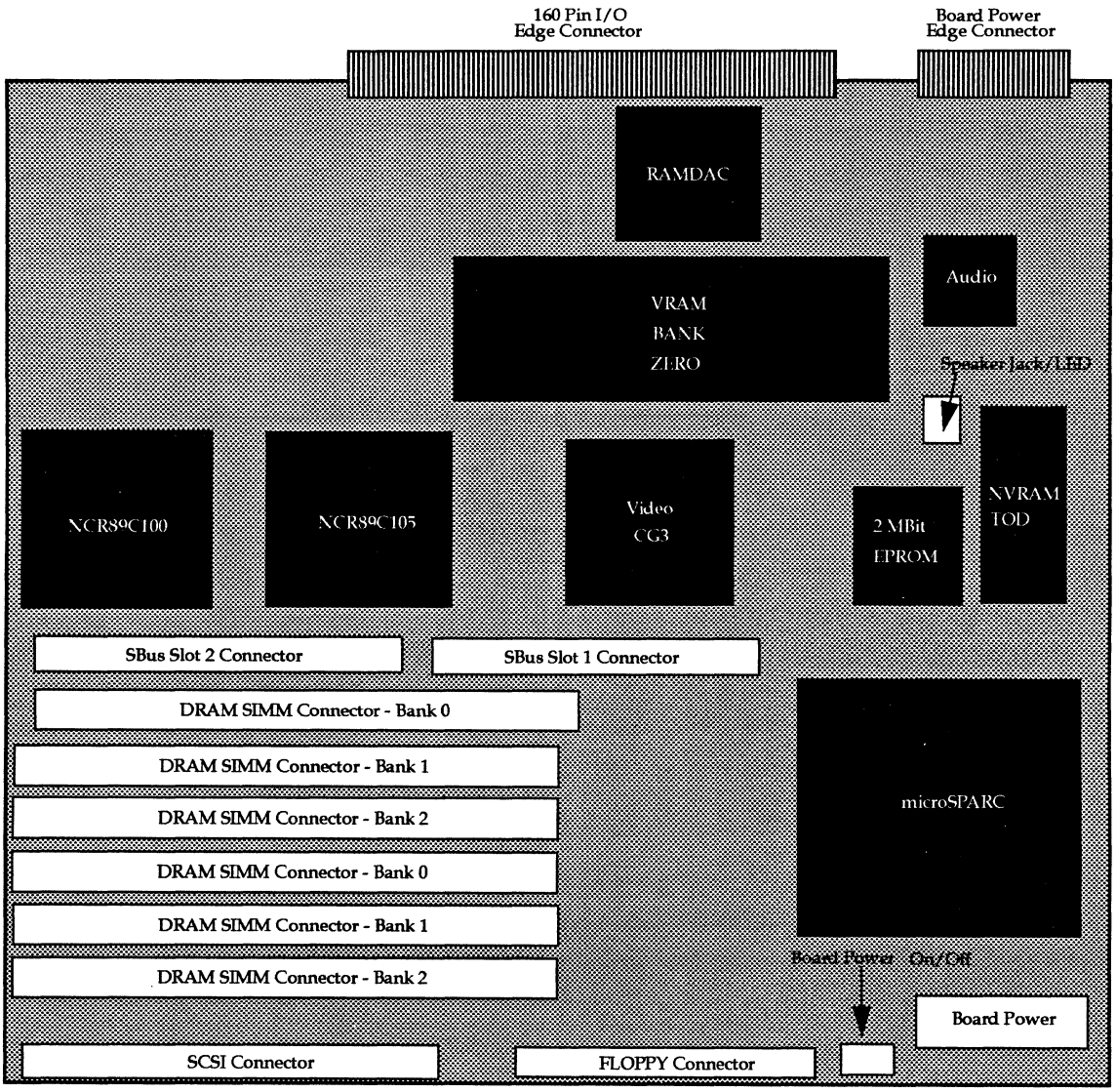
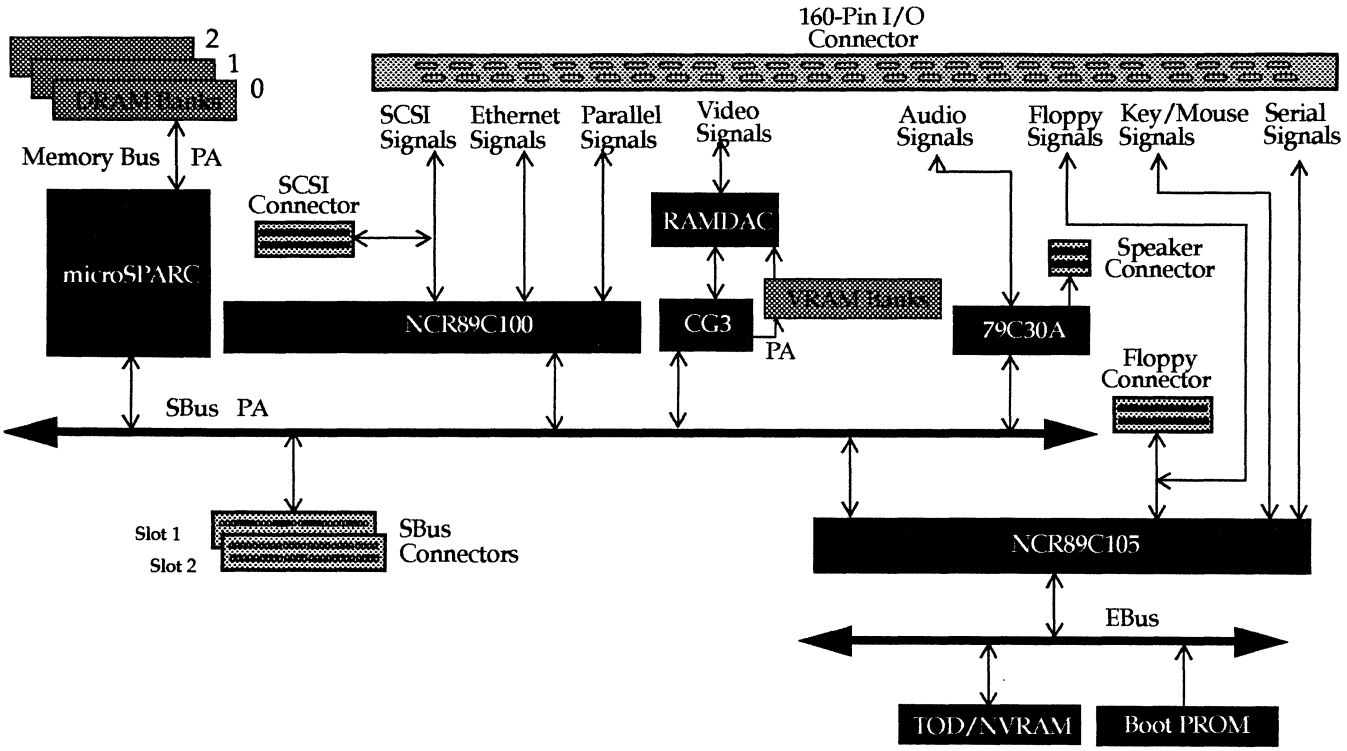
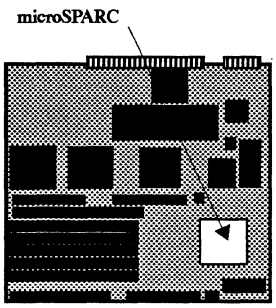


Figure 5-2 High-Level Block Diagram of the SPARCclassic Engine Board



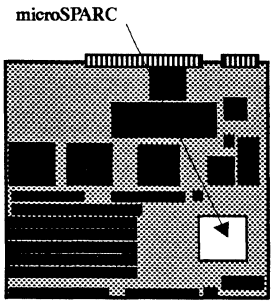
5.2 *Main Components*

5.2.1 *microSPARC Microprocessor*



microSPARC is a single-chip microprocessor containing an Integer Unit, a Floating Point Unit, data and instruction caches, Memory Management Unit, and controllers for Main Memory Cache, Random-Access Memory, Direct-Memory Access, and SBus.

microSPARC runs at 50 MHz, with a processing speed of up to 59.1 million instructions per second (MIPS). The FPU runs at 4.6 million floating-point operations per second (MFLOPS). Performance measurement configuration is defined in **Chapter 4**.



Integer Unit (IU) and Floating-Point Unit (FPU)

The basic core of the microSPARC is the combined SPARC Integer Unit/ Floating-Point Unit (IU/FPU). The IU/FPU's clock speed is 50 MHz.

The IU includes a 32-bit bus interface with separate data and address instruction buses, a five-stage instruction pipeline, a barrel shifter, two data aligners, and a three-port register file consisting of 128 registers. These registers are configured into overlapping sets that facilitate the passing of parameters. All instructions with the exception of load doubles, stores, and floating-point operations can be executed in one machine cycle.

Main Memory Cache

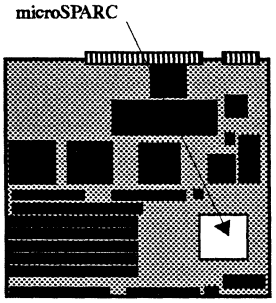
Cache memory included in the microSPARC chip provides high-speed local memory for the IU. The 2 KB data cache is a direct-mapped physical-address write-through cache with no write allocate, organized with 128 lines of 16 bytes of data. The 4 KB instruction cache is a physically-addressed cache, organized with 128 lines of 32 bytes of data.

Reference Memory Management Unit (MMU)

The SPARC Reference Memory Management Unit (SRMMU) contains clock generation logic and the MMU data path/decode logic. It is connected to the SBus. The SRMMU implements virtual memory. The SRMMU maps the virtual addresses used by user programs, operating system kernel, and input/ output devices to physical memory addresses. Virtual memory allows a user program to have access to an address space that is larger than the physical memory present on the system.

The MMU isolates the address space of one process from that of another, preventing errors in a user-level program from bringing the entire system down. It also controls the protections (read-only or read/write) associated with each page of memory, allowing, for example, one copy of a shared library to be used by many running programs.

The CPU board architecture is divided between control space and device space. Control space contains the architectural extensions to the CPU, on the untranslatable side (VA) of the MMU. Device space contains the devices on the translated side (PA) of the MMU. Control space is used for system control operations, and device space is used (mostly) for normal operation.



The MMU translates the virtual address output of the CPU and drives the resultant physical address onto the SBus. It also decodes this physical address into a set of select signals used to enable the main memory and I/O devices on the SBus. The MMU supports I/O translations for DVMA between SBus devices and the main memory.

Translation Lookaside Buffer (TLB)

The TLB is 32-entry fully-associative translation-lookaside buffer that uses a pseudo-random algorithm for the replacement of page table entries.

RAM Controller

The Random Access Memory (RAM) controller provides control over the available DRAM. The RAM controller uses 60 nsec DRAMs to give burst reads and writes at two words per clock. It also provides parity generation and checking. The RAM controller has a private RAM data bus, isolating the DRAM data from the SBus data. This lowers the load on the SBus data lines, in addition to allowing the RAM controller to do buffered writes while releasing the SBus.

SBus Controller

The 25 MHz SBus (controlled by microSPARC) is the basic communication mechanism between the processing core (CPU), the MMU, and the main memory and various I/O devices, including SBus devices operating out of the three virtual SBus slots and the two physical SBus slots.

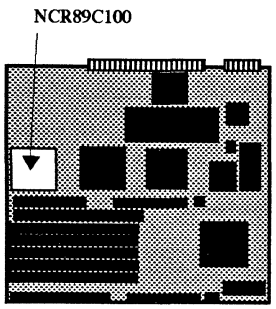
Table 5-1 SPARCclassic Engine SBus Slots

SBus Slot Number	Function of SBus Slot
Slot 0	Physical SBus slot 0 for an SBus Card
Slot 1	Physical SBus slot 1 for an SBus Card
Slot 2	Not Used
Slot 3	Sun CG3 Video
Slot 4	I/O

5.2.2 *Input/Output Controllers & 8-Bit Devices*

NCR89C100 (Master I/O Controller)

All DVMA or SBus master input and output is controlled by a Sun Microsystems ASIC called NCR89C100.



Ethernet Controller Macrocell

Ethernet is supported by a Local Area Network Controller for Ethernet (LANCE-compatible subsystem) within the NCR89C100 chip. The Ethernet signals are brought to the 160-pin I/O connector in two forms: AUI (thick net) or twisted-pair. Only one Ethernet channel is provided, so only one may be used at any one time. The Ethernet driver defaults to the AUI connector if both sets of signals are active simultaneously. The Boot PROM is auto-sensing.

SCSI Controller Macrocell

SCSI device operations are handled through a SCSI controller macrocell (FAS101-compatible) within the NCR89C100 chip. All SCSI devices interface to the SBus through the DMA controller, also contained within NCR89C100.

DMA Controller Macrocell

Direct-Memory Access (DMA) is handled through the DMA2 controller macrocell within NCR89C100. It has three external interfaces designed to provide DMA access to Ethernet, SCSI, and a Centronics-type parallel port.

The direct memory access (DMA2) has internal line buffers and does SBus burst operations of 16 bytes at a time (where possible) in order to minimize SBus usage.

The DVMA (Direct Virtual Memory Access) function, performed by the DMA Controller, provides two channels of direct memory access between the SCSI port. parallel port, and Ethernet port interfaces.

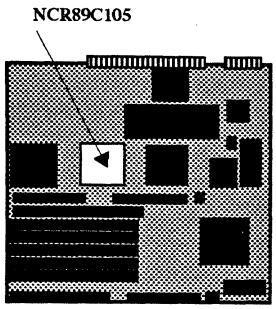
DVMA also provides the path between the SBus and the SCSI and Ethernet interface devices required for the IU to initialize and configure these interfaces.

Printer Port Controller Macrocell

Centronics-compatible parallel port operations are handled through the DMA2 controller macrocell within NCR89C100.

NCR89C105 (Slave I/O Controller)

All slave SPARCclassic Engine inputs and outputs are controlled by one ASIC called NCR89C105.



Serial Port A Controller

Serial port A is provided to connect with peripheral equipment such as terminals, printers, and modems. RS232 only, asynchronous or synchronous.

Serial Port B Controller

Serial port B is provided to connect with peripheral equipment such as terminals, printers, and modems. RS232 only, synchronous only.

Keyboard/Mouse Controller

The Sun Microsystems standard keyboard/mouse ports are provided to connect with a Sun-compatible keyboard and mouse.

Floppy Disk Drive Controller

This is an industry standard 3 1/2" internal floppy interface.

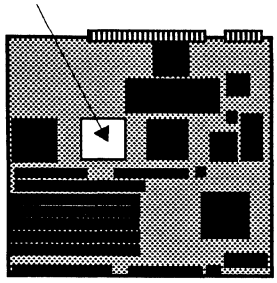
EBus Controller

Circuitry is included that controls a special internal bus for the NCR89C105 ASIC called the EBus (Sun Microsystems Expansion (or Eight-Bit) Bus). The EPROM and NVRAM/TOD are the devices controlled by this EBus.

Power Up/Power Down Controller

Circuitry is included to power up and down the CPU board/system, as defined by your own configuration. In a workstation configuration, the power-on is provided by the keyboard, and the power-off is software controllable.

NCR89C105



JTAG Internal & Boundary Scan Controller

Signal paths and circuitry are provided to perform a ASIC-level diagnostic examination of NCR89C105.

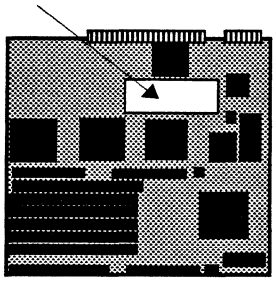
Interrupt Controls

NCR89C105 contains a uni-processor subset of the Sun-4M interrupt controller. It contains all system logic and a single set of processor-specific circuitry, with 15 levels of software-generated and/or externally-generated interrupts. Assignment and prioritization of these interrupts is performed by the interrupt logic.

System Reset Controls

Circuitry is provided to control system resets. There are two sources of reset recognized by the system reset controller: Power-on Reset (POR) and Software Reset (SWR). Either of these two sources will cause NCR89C105 to assert a reset signal, which returns the SPARCclassic Engine board to a known state. It is not possible to reset part of the system and leave the rest untouched via these two resets.

VRAM



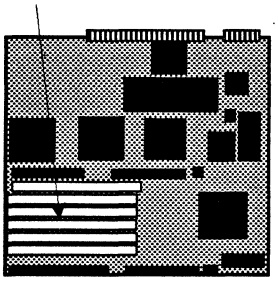
Counter/Timer Controls

NCR89C105 features two programmable counter/timer channels, compatible with the timers specified in the Sun-4M specification. NCR89C105 implements only the system portion and a single processor-specific set of timers. Various operational modes are available.

Slot 0 Video RAM (VRAM)

The VRAM for slot 0 is soldered to the board.

DRAM Connectors



Single Inline Memory Modules (DRAM SIMMs)

4 MB or 16 MB SIMMs can be used in the six SPARCclassic Engine SIMM slots. Main memory can be expanded up to 96 MB.

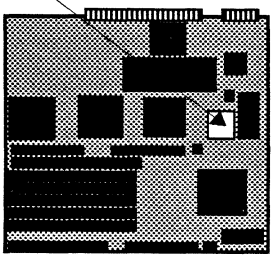
Because SPARCclassic Engine memory is 64 bits wide, SIMMS must be added in pairs, and with similar-sized SIMMS. 1, 2, 4, 8, and 16 byte accesses are supported by microSPARC.

SPARCclassic Engine is designed to use 4MB or 16 MB 60 nsec Sun Microsystems non-standard 33 bit SIMMs that supports a single parity bit per 32 bit word.

A standard SIMM can be used with SPARCclassic Engine. When used with the SPARCclassic Engine, three of the standard SIMM parity DRAM chips remain unused.

Open Boot PROM (OBP)

Boot PROM



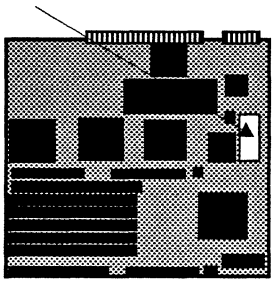
The Open Boot PROM is connected to the Sun Microsystems Expansion Bus (EBus). The OBP is 256 K x 8 (2 Mbit) in size and contains the boot code, diagnostics, and the FORTH Toolkit.

The OBP does the following:

- Runs start-up diagnostic tests.
- Initializes the host machine.
- Reads non-volatile RAM (NVRAM) and executes the boot sequence. Usually, this consists of booting SunOS. In some cases, however, the Diagnostic Executive or standalone programs can also be run.
- Supplies program code for the abbreviated system monitor. Entry into the system monitor is signified by the > prompt. If a boot attempt fails, the Open Boot PROM tries to start the abbreviated system monitor.
- Supplies program code for the FORTH Toolkit, the on-CPU board diagnostics contained the FORTH Toolkit, and the FORTH language interpreter. Entry into the FORTH Toolkit is signified by the `ok` prompt.
- Supports byte, halfword, and word accesses.

Non-volatile RAM (NVRAM)

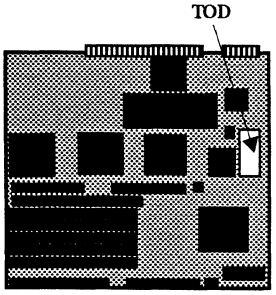
NVRAM



The NVRAM chip is 8 KB of non-volatile Random Access Memory (NVRAM). The NVRAM chip is connected to the EBus. A single lithium battery within the NVRAM module provides battery backup for the NVRAM.

The NVRAM stores the default system configuration parameters. You can modify these parameters using the FORTH Toolkit in the OBP.

The NVRAM chip also contains the Time-of-Day Clock (see below).

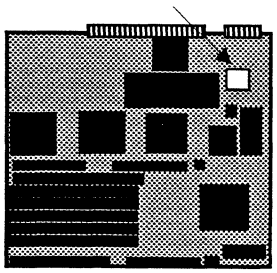


Time-of-Day Clock (TOD)

The NVRAM chip contains the time-of-day clock (TOD). The TOD chip is connected to the EBus. A single lithium battery within the NVRAM module provides battery backup for the TOD.

JTAG Support

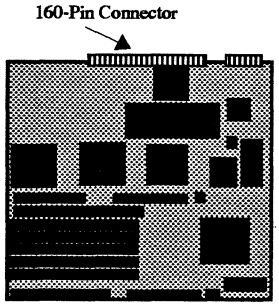
The SPARCclassic Engine board supports the Joint Test Action Group (JTAG) scan-loop testability scheme in the microSPARC, NCR89C100 and NCR89C105 ASICs. The pins that make up the JTAG control signals for the scan loops are brought out to the 160-pin I/O edge connector (see **SPARCclassic Engine Board Connectors** below).



Audio Controller

The SPARCclassic Engine board uses the Am79C30A Digital Subscriber Controller (DSC) as a standard 8-bit voice monophonic audio controller (ISDN is not supported on the SPARCclassic Engine). The audio processor in the Am79C30A uses Digital Signal Processing (DSP) to implement the CODEC and filter functions. The audio processor interfaces to a speaker, headphone, and two separate audio inputs.

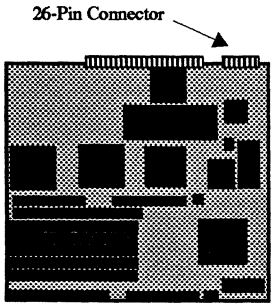
5.2.3 *SPARCclassic Engine Board Connectors*



160-Pin I/O Male Edge Connector

A male 160-pin edge connector is the major I/O connector on the SPARCclassic Engine board. In a workstation configuration, the I/O connector provides the signals to the SPARCclassic I/O board's 160-pin shielded female connector, enabling the I/O connectors on that board. In an OEM configuration, the 160-pin connector could be used directly as the I/O connector, the SPARCclassic I/O board could be used to supply I/O connectors, or an I/O board of your own design could be used to implement selected I/O ports.

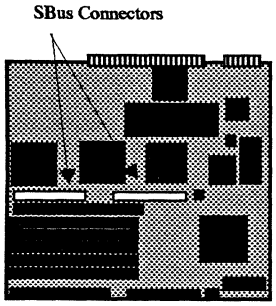
The 160-pin male edge connector has all signals for the SPARCclassic Engine board except for the SBus signals. Therefore, this also is a good test interface for the board for troubleshooting.



JTAG scanning on the SPARCclassic Engine board is accomplished through the appropriate pins on the 160-pin edge connector. microSPARC, DBRI, NCR89C100 and NCR89C105 are capable of JTAG troubleshooting.

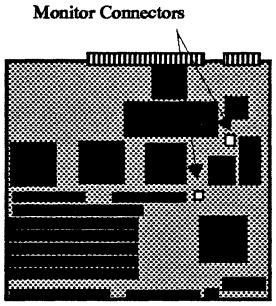
26-Pin Power Male Edge Connector

The power edge connector contains the power signals for the SPARCclassic Engine board routed to the edge for testing purposes only. This connector is available to be used as the main power connector, if you can make use of it in your design.



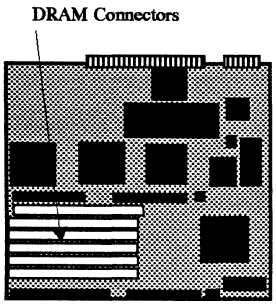
SBus Slot (SBus Devices) Female Connectors

There are two 25 MHz physical SBus 96-pin high-density female connectors on the SPARCclassic Engine board. The SBus slots connect to the SBus data bus and the SBus address bus. The SBus is an open systems 32-bit synchronous bus with a 28-bit address space and the connectors can be used for any available SBus board. The physical slots have full master/slave capabilities. Additional mechanical support must be provided in your enclosure design for the SBus cards, as defined in the SBus specifications. Future Sun Microsystems video SBus cards will support keyboard/mouse control of the monitor. These SBus cards will have a cable that connects to the monitor control pins adjacent to each of the SBus slots (see **4-Pin Monitor Connectors** below).



4-Pin Monitor Connectors

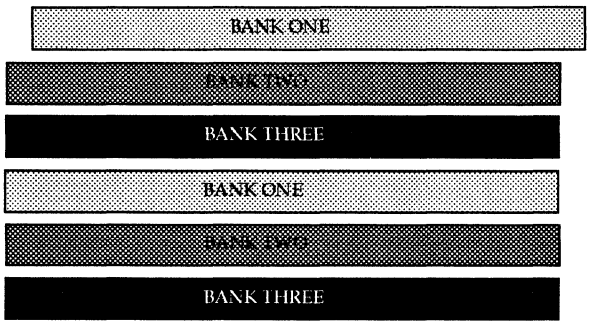
There are two 4-pin Monitor Port connectors on the SPARCclassic Engine board, one for each SBus slot. A cable from a future Sun Microsystems SBus video card would connect with the associated 4-pin Monitor Port connector to provide keyboard control of the monitor.

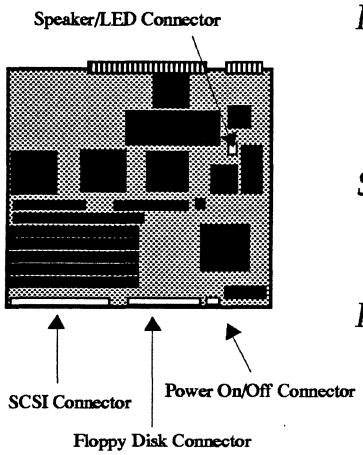


Main Memory DRAM SIMM Female Connectors

DRAM SIMM slots 1 through 6 are the main memory. 1, 2, 4, 16, and 32 MB SIMMs can be used in these slots (both Sun Microsystems non-standard SIMMs or industry-standard SIMMs). Size of the SIMMs cannot be mixed within a bank. There are three banks (two slots each). The bank pattern is shown in the diagram below:

Figure 5-3 DRAM SIMM Bank Pattern





Floppy Disk Drive Female Connector

The floppy disk drive industry-standard connector can be used for any floppy disk drive.

SCSI Female Connector

This 50-pin dual-row SCSI connector can be used for any SCSI device.

Power On/Off Connector

A three-pin connector on the SPARCclassic Engine board that connects via a cable to the power supply (Sun Microsystems configuration). The intent (for Sun Microsystems) is to have a Type-5 Sun Microsystems keyboard generate a signal that is interpreted as a power-on signal when the system is off, and a power-off signal when the system is on. There is no restriction on possible different uses of these signals in a design of your choosing, when you do not have a Sun Microsystems Type-5 keyboard in your design.

Speaker/LED Male Connector

This 4-pin connector is provided to provide monophonic sound output to a small workstation speaker and a single CPU status LED.

5.3 System Considerations

5.3.1 Required Initial Power-Up System Components

- a power supply
- a AC power-supply power cord (to power source)
- a power-supply power cable (to SPARCclassic Engine)
- an ASCII terminal connected:
  - a terminal keyboard
  - an AC terminal power cord
  - a terminal communications cable to SPARCclassic Engine serial port A

5.3.2 System Expansion Components

A small monophonic speaker, a floppy disk drive, SCSI device(s), and various SBus cards (including video SBus cards, Ethernet SBus cards, etc.) can be added directly to the SPARCclassic Engine. There are many variations of equipment possible to connect directly to SPARCclassic Engine.

Other devices can be connected to the SPARCclassic Engine board via the SPARCclassic I/O board. These include speakers, headphones, microphones, monitors, keyboards, mice, additional SCSI devices, audio control boxes, parallel printers, and Ethernet.

All additional components must be purchased separately.

5.3.3 Required Enclosure

The SPARCclassic Engine board must be mounted into a chassis of your design. Other than the physical form factor, environmental factors (cooling requirements and moisture/height limitations), SBus card single-height form factors, and impact limitations, there are no required enclosure specifications.

It is recommended that the height of an SBus card with the SPARCclassic Engine is included in your design, even though it may not be required by the immediate application specifications, to allow for future expansion of the capabilities of your design for future needs.

For initial test purposes in a laboratory setting, no enclosure is required. However, be extremely careful of the TAB mounting of the microSPARC, as it is quite fragile and can be ruined by electrostatic discharge (ESD).

5.3.4 *The SPARCclassic I/O Board*

The 160-pin I/O male edge connector at the back of the SPARCclassic Engine board can be mated to the SPARCclassic I/O board to expand the I/O connectors to a full-workstation configuration (see **Appendices G, H, I, and J** for information on the SPARCclassic I/O board).

Removal & Replacement Procedures 6

6.1 Before You Begin

Before you begin to replace CRUs, make sure you do the following:

- Halt your system
- Gather the proper tools
- Disconnect external peripherals (if any)
- Open the enclosure (if any)
- Attach an ESD wrist strap

Caution – Printed circuit boards are made of delicate electronic components that are extremely sensitive to static electricity. Ordinary amounts of static from your clothes or work environment can destroy the boards. Handle boards only by the non-conducting edges. Do not touch the components themselves or any metal parts. Always wear a grounding (wrist) strap when handling the boards. Attach the wrist strap to the metal casing of the power supply at the rear of the unit top.

Caution – The AC power cord should remain attached between the system unit and an AC wall outlet. This connection provides the ground path necessary to protect internal system components from harmful static discharges. Inside the system unit, be sure the power supply wiring harness is connected to the main logic board to complete the ground.

Warning - Verify that the system power switch is in the Standby (⏻) position. The green LED at the front of the system unit should not be lit and the fan should not be running.

Warning - When the system power switch is in the Standby (⏻) position, and the AC power cord remains connected to a power outlet, hazardous AC voltage is still present in the power supply primary. Do not attempt to service the power supply under these conditions. Disconnect the AC power cord prior to handling the power supply. When servicing any other system component, the AC power cord should remain connected and poses no safety hazard.

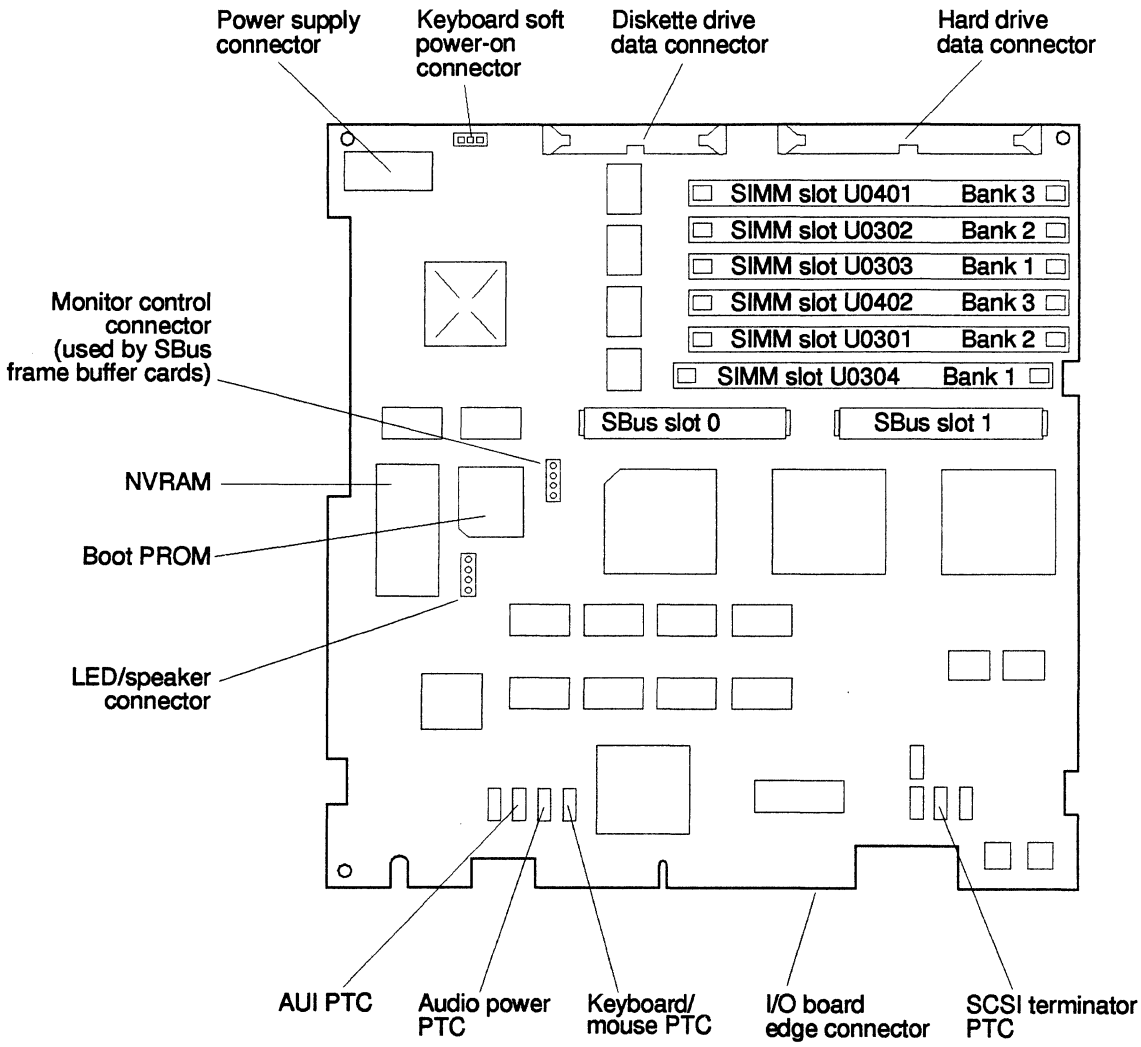


Figure 6-1 Board Layout—SPARCclassic Engine

6.2 *Turning Off the Power*

Before you begin any removal/replacement procedure, you must halt the system in an orderly manner. The procedure depends on whether your system is working normally or not.

Note – This section assumes that you are running Solaris. If you are running a non-Sun Microsystems operating system, refer to the documentation that accompanies it and halt your system according to the instructions therein.

Caution – When the operating system or any other stand-alone program has already booted, do not use the Stop(L1)-a keys to halt the system. Using the Stop(L1)-a keys to abort program execution may cause damage to data files.

6.2.1 *When Your System is Working Normally*

To halt your system when it is working normally:

1. **Save all your work.**
   Consult your software documentation for instructions on ending a work session and saving your files. If you do not save your work, you could lose it when you switch off the power.

2. **Return to the operating system environment.**
   If you are in a windowing environment, exit from it and wait for the system prompt to appear. See the documentation supplied with your windowing system.

3. **Halt the operating system.**
   See the documentation supplied with your operating system for instructions on how to halt it.

   For example, if you are using the Solaris® 2.x operating system:

   a. At the system prompt, type `su` and press Return.

   b. Type your superuser password and press Return.

   c. Type `/usr/sbin/halt` and press Return.

```
nevada% su
Password: welcome      (Password does not appear on screen.)
nevada# /usr/sbin/halt
```

4. **After halting the operating system, wait for either the > or ok prompt.**
   The system displays system halt messages followed by either the > or ok prompt.

   When either prompt appears, you can safely turn off the power in the proper sequence.

5. **Turn off the power in this order:**
   External drive units (if you have any)
   System unit
   Monitor

6.2.2 *When Your System Does Not Respond Normally*

To halt a system that is hung, or frozen, and unresponsive to commands:

1. **If your system is on a network, wait a few minutes before proceeding.**
   Your system's slow response may be due to network problems or delays. Check with the person in charge of your network. If the response is not due to the network, go to the next step.

2. **Press Stop(L1)-a (or Break).**
   If you use a Wyse® WY-50™, VT100™, or compatible terminal as the console with your SPARCstation system unit, press Break instead of Stop(L1)-a.

   Pressing Stop(L1)-a (or Break) puts the system into the PROM monitor command mode (indicated by the ok prompt).

Note – If the system does not respond to the mouse and keyboard, pressing Stop(L1)-a will not be effective. You may have to turn the power off, wait at least 10 seconds, and turn the power on again. Then try pressing Stop(L1)-a once more.

---

3. **When the ok or > prompt appears, boot the operating system.**
   Type boot at the ok prompt or b at the > prompt.

4. **When you see the `login` prompt, login to the system with your user name and password.**

5. **Halt the operating system.**
   See the documentation supplied with your operating system for instructions on how to halt it.

   For example, if you are using the Solaris® 2.x operating system:

   a. At the system prompt, type `su` and press Return.

   b. Type your superuser password and press Return.

   c. Type `/usr/sbin/halt` and press Return.

```
nevada% su
Password: welcome      (Password does not appear on screen.)
nevada# /usr/sbin/halt
```

6. **After halting the operating system, wait for either the > or `ok` prompt.**
   The system displays system halt messages followed by either the > or `ok` prompt.

   When either prompt appears, you can safely turn off the power in the proper sequence.

7. **Turn off the power in this order:**
   External drive units (if you have any)
   System unit
   Monitor

6.3 *Attaching a Wrist Strap*

A *wrist strap* (or *grounding strap*) provides grounding for static electricity between your body and the chassis of the system unit. Electric current and voltage do not pass through the wrist strap. Before you handle any components inside the SeEC, attach the wrist strap to your wrist and to the metal casing of the power supply. Parts that require the use of a wrist strap are packed with one.

Caution – Boards and modules can be damaged by harmful electrical charges if you do not wear a wrist strap.

To attach the wrist strap:

1. **Wrap the grounding strap twice around your wrist.**
   Make sure the adhesive side is against your skin.
2. **Attach the end with the adhesive copper strip to the metal casing of the power supply in the top of the system unit.**

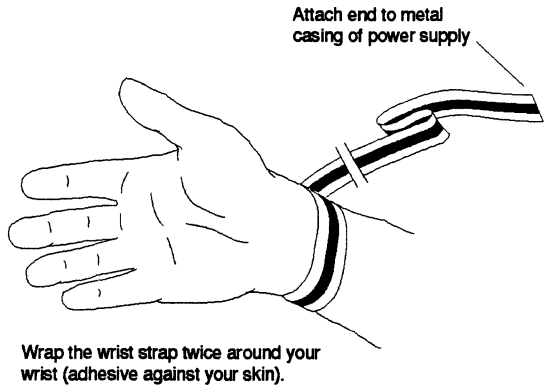


Figure 6-1 Attaching a Wrist Strap

6.2 *DSIMM Removal & Replacement*

This section explains how to remove & replace DSIMMs in a SPARCengine EC.

Caution – DSIMMs installed in your system must be specifically designed to operate in it. *Do not* remove DSIMMs from a different Sun system and install them in a SPARCengine EC.

The SPARCclassic Engine contains six DSIMM slots capable of accepting either 4-megabyte or 16-megabyte DSIMMs. The six DSIMM slots are logically grouped into three memory banks, with two DSIMM slots to a bank. Each slot is labeled 1, 2, or 3 to indicate its corresponding memory bank.

You can combine 4-megabyte DSIMMs with 16-megabyte DSIMMs in the same system, but you must observe the following restriction: The two DSIMM slots within each bank must be identically configured (i.e., they should both contain the same type of DSIMM or else both should be empty).

This section describes the procedures for removing and replacing faulty DSIMMs.

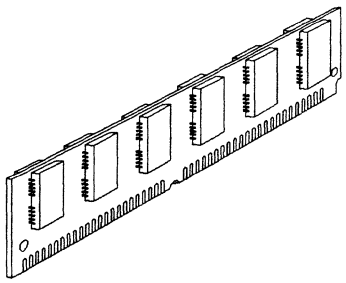


Figure 6-1 Typical DSIMM

Figure 6-2 shows the DSIMM slot locations on the main logic board. Table 6-1 shows the configuration matrix for memory modules. The maximum memory configuration is 96 megabytes using six 16-megabyte DSIMMs.

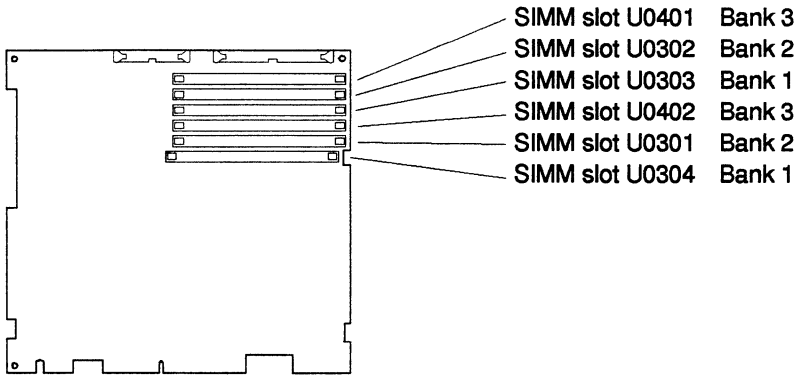


Figure 6-2 DSIMM Slot Locations

Table 6-1 Configuration Matrix for Memory Modules

Total Memory	Slot U0304	Slot U0301	Slot U0402	Slot U0303	Slot U0302	Slot U0401
16 MB	4 MB	4 MB	—	4 MB	4 MB	—
24 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB
32 MB	16 MB	—	—	16 MB	—	—
40 MB	16 MB	4 MB	—	16 MB	4 MB	—
48 MB	16 MB	4 MB	4 MB	16 MB	4 MB	4 MB
64 MB	16 MB	16 MB	—	16 MB	16 MB	—
72 MB	16 MB	16 MB	4 MB	16 MB	16 MB	4 MB
96 MB	16 MB	16 MB	16 MB	16 MB	16 MB	16 MB

6.2.1 *Determining Faulty DSIMM Locations*

The Sundiag System Exerciser, SunDiagnostic Executive, and the POST diagnostics can report memory errors encountered during program execution. Memory error messages on the video monitor usually indicate a physical memory address where the error was detected.

Depending on the diagnostic program you are running, a DSIMM location number ("U" number) may be displayed. If the location number is present in the error message, follow the instructions later in this chapter for removing the defective DSIMM at that location and installing a replacement.

If a location number is not displayed but a physical memory address is shown, locate the DSIMM slot containing the defective DSIMM. First, see which memory bank contains the physical address. Then, look up the last digit of the address to find out which of the two DSIMMs in that bank caused the memory error.

For example, if an error is detected at physical memory address 12fe958, the error occurred in memory bank 1 (DSIMMs U0304 and U0303). The defective DSIMM is in slot U0304. Follow the instructions later in this chapter for removing the defective DSIMM at that location and installing a replacement.

Table 6-1 Physical Memory Address Range of Memory Banks *

Bank	SIMM #	Physical Memory Address Range 4MB SIMMs	16MB SIMMs
1	U0304	0000000 *through* 07FFFFF	0000000 *through* 1FFFFFF
1	U0303	0000000 *through* 07FFFFF	0000000 *through* 1FFFFFF
2	U0301	2000000 *through* 27FFFFF	2000000 *through* 3FFFFFF
2	U0302	2000000 *through* 27FFFFF	2000000 *through* 3FFFFFF
3	U0402	4000000 *through* 47FFFFF	4000000 *through* 5FFFFFF
3	U0401	4000000 *through* 47FFFFF	4000000 *through* 5FFFFFF

* Both DSIMMs in a memory bank have the same physical address range. The last digit in the physical address determines which of the two DSIMMs in a bank caused the memory error (see Table 6-2).

Table 6-2 Determining the Defective DSIMM

If the physical address ends in:	The defective DSIMM is in:
0, 1, 2, 3, 8, 9, A, or B	U0304, U0301, or U0402
4, 5, 6, 7, C, D, E, or F	U0303, U0302, or U0401

6.2.2 *Removal of a DSIMM*

The procedure for removing a DSIMM is the same for 4-megabyte and 16-megabyte DSIMMs.

Caution – Printed circuit boards are made of delicate electronic components that are extremely sensitive to static electricity. Ordinary amounts of static from your clothes or work environment can destroy the boards. Handle boards only by the edges. Do not touch the components themselves or any metal parts. Always wear a grounding (wrist) strap when handling the boards. Attach the wrist strap to the metal casing of the power supply at the rear of the unit top.

Caution – The AC power cord should remain attached between the system unit and an AC wall outlet. This connection provides the ground path necessary to protect internal system components from harmful static discharges. Inside the system unit, be sure the power supply wiring harness is connected to the main logic board to complete the ground.

Warning – Verify that the system power switch is in the Standby (⏻) position. The green LED at the front of the system unit should not be lit and the fan should not be running.

Warning – When the system power switch is in the Standby (⏻) position, and the AC power cord remains connected to a power outlet, hazardous AC voltage is still present in the power supply primary. Do not attempt to service the power supply under these conditions. Disconnect the AC power cord prior to handling the power supply. When servicing any other system component, the AC power cord should remain connected and poses no safety hazard.

To remove a 4-megabyte or 16-megabyte DSIMM:

1. **Locate the DSIMM slots on the main logic board.**

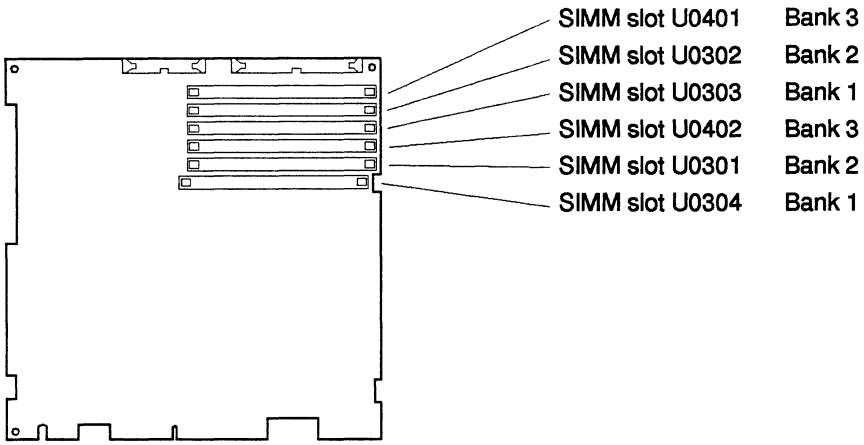


Figure 6-1 DSIMM Slot Locations

Table 6-1 Configuration Matrix for Memory Modules

Total Memory	Slot U0304	Slot U0301	Slot U0402	Slot U0303	Slot U0302	Slot U0401
16 MB	4 MB	4 MB	—	4 MB	4 MB	—
24 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB
32 MB	16 MB	—	—	16 MB	—	—
40 MB	16 MB	4 MB	—	16 MB	4 MB	—
48 MB	16 MB	4 MB	4 MB	16 MB	4 MB	4 MB
64 MB	16 MB	16 MB	—	16 MB	16 MB	—
72 MB	16 MB	16 MB	4 MB	16 MB	16 MB	4 MB
96 MB	16 MB	16 MB	16 MB	16 MB	16 MB	16 MB

2. **Place an antistatic mat, shiny side up, next to the system unit.** The mat is supplied with the replacement DSIMMs.
3. **Make sure the wrist strap is securely attached to your wrist and to the metal casing of the power supply.**

4. **Locate and remove the faulty DSIMM.**
   The DSIMMs are held in their slots by metal clips. To release the modules, pry apart the clips with your fingernails while pushing the top of the module gently forward about 30 degrees from the vertical position. Then pull the DSIMM out of its socket.

   Any DSIMMs you remove should be placed on the antistatic mat.

Note – The DSIMMs are closely spaced. In order to remove a DSIMM, you may find it necessary to remove adjacent DSIMMs first. Keep track of which DSIMMs are installed in which slots. If you are removing a defective DSIMM, take care not to get it mixed up with the other DSIMMs.

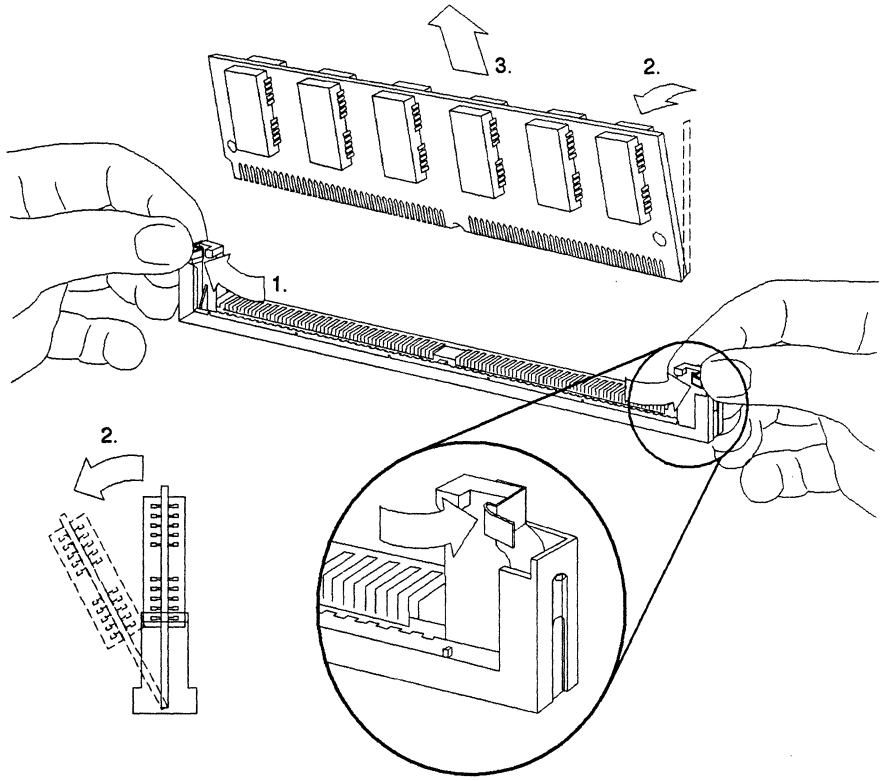


Figure 6-2 Removing a DSIMM

6.2.3 *Inserting a DSIMM*

To install a DSIMM:

Caution – The SIMMs installed in your system must be specifically designed to operate in it. *Do not* transfer a SIMM from a different Sun system unless you are sure it is compatible with your system.

Warning – Verify that the system power switch is in the Standby (⏻) position. The green LED at the front of the system unit should not be lit and the fan should not be running.

Warning – When the system power switch is in the Standby (⏻) position, and the AC power cord remains connected to a power outlet, hazardous AC voltage is still present in the power supply primary. Do not attempt to service the power supply under these conditions. Disconnect the AC power cord prior to handling the power supply. When servicing any other system component, the AC power cord should remain connected and poses no safety hazard.

1. **Locate the DSIMM slots on the main logic board.**
2. **Make sure the wrist strap is securely attached to your wrist and to the metal casing of the power supply.**
3. **Remove each DSIMM from its protective packaging and place it on an antistatic surface.**
   The bag that the DSIMM is packed in makes a good antistatic surface.
4. **Determine where to install the new DSIMMs.**
5. **See the configuration matrix in 6-4. You may need to relocate existing DSIMMs to match one of the configurations below SIMM Configurations Matrix.**

Caution – The four DSIMM slots are logically grouped into two memory banks—labeled 1 and 2 (see Figure 6-3). When installing DSIMMs, you must make sure that the two DSIMM slots within each bank are identically configured (i.e., both slots should contain the same type of DSIMM or else both should be empty).

6. **Remove any DSIMMs that must be relocated.**
   The DSIMMs are held in their slots by metal clips. To release a DSIMM, pry open the clips with your fingernails while pushing the top of the module gently forward about 30 degrees from the vertical position (see Figure 6-3). Then pull the DSIMM out of its socket and place it on the antistatic surface.

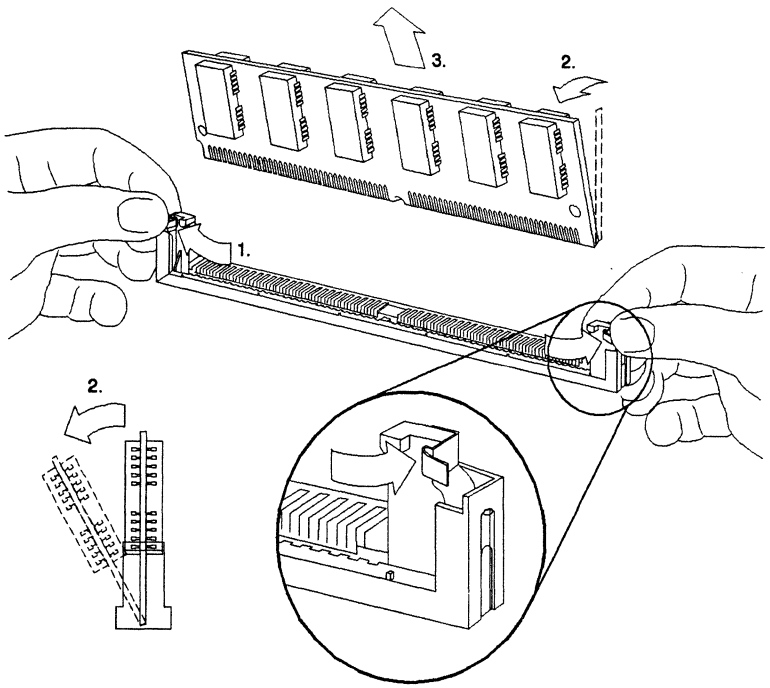


Figure 6-3 Removing a DSIMM

Note - The DSIMMs are closely spaced. In order to remove a DSIMM, you may find it necessary to remove adjacent DSIMMs first. Keep track of which DSIMMs should be installed in which slots.

7. **Install the new DSIMMs and any others you may have removed.**
   Since the DSIMMs are closely spaced, they must be installed in the proper order. Start with the slot closest to the center of the main logic board and work outward toward the board's front edge.

   Hold each DSIMM at its edges and insert it into the plastic guides at an angle about 30 degrees from the vertical position (see the figure below). Then, by pushing gently on its top edge, rotate the DSIMM into an upright position. You should hear it click into place.

Note - Each DSIMM is keyed so it can only be installed in one way.

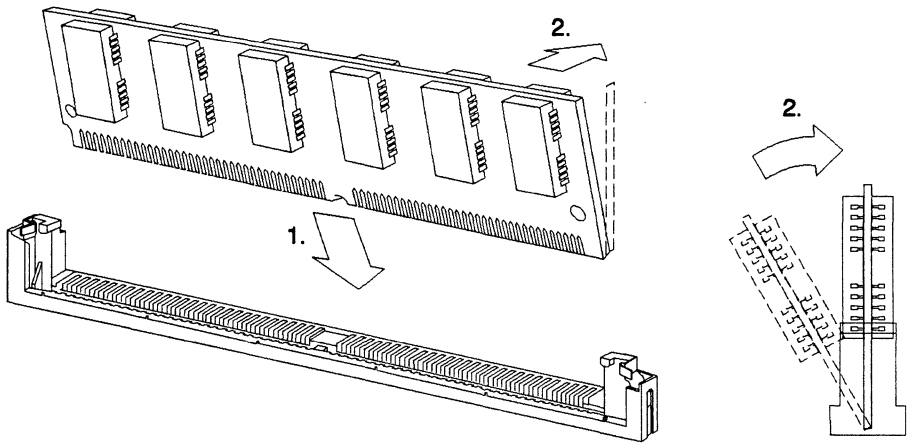


Figure 6-4 Installing a DSIMM

6.5 SBus Cards

This section describes the procedures for removing and replacing a faulty SBus card.

6.5.1 Removing SBus Cards

To remove an SBus card from the system unit:

1. **Prepare to work on the system.**
   Halt the system and verify that the power is off. Then open any enclosure and attach a wrist strap.

Caution – The AC power cord should remain attached between the system unit and an AC wall outlet. This connection provides the ground path necessary to protect internal system components from harmful static discharges. Inside the system unit, be sure the power supply wiring harness is connected to the main logic board to complete the ground.

Warning – Verify that the system power switch is in the Standby (⏻) position. The green LED at the front of the system unit should not be lit and the fan should not be running.

Warning – When the system power switch is in the Standby (⏻) position, and the AC power cord remains connected to a power outlet, hazardous AC voltage is still present in the power supply primary. Do not attempt to service the power supply under these conditions. Disconnect the AC power cord prior to handling the power supply. When servicing any other system component, the AC power cord should remain connected and poses no safety hazard.

2. **Place the antistatic mat, shiny side up, next to the SeEC.**
   The mat is supplied with the replacement SBus card.
3. **Detach any external cables connected to the faulty SBus card (if applicable)**
4. **Detach any internal cables leading from the SBus card to the SeEC (if applicable).**
   Detach the cables from their connectors on the main logic board.

5. **Remove the faulty SBus card.**
   Place your index fingers or thumbs beneath the corners of the SBus card where it plugs into its slot. Lift up on the card to release it from the slot.

Caution – The plastic SBus card retainer is not a handle. Pulling on the SBus card retainer can cause it to break.

6. **Place the SBus card on an antistatic mat.**

6.5.2 *Replacing SBus Cards*

Warning – Verify that the system power switch is in the Standby (⏻) position. The green LED at the front of the system unit should not be lit and the fan should not be running.

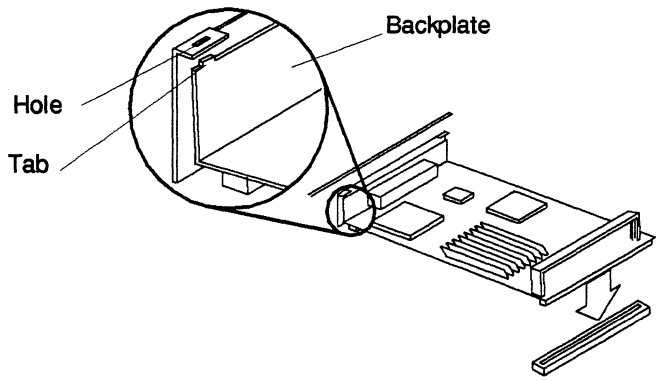
Warning – When the system power switch is in the Standby (⏻) position, and the AC power cord remains connected to a power outlet, hazardous AC voltage is still present in the power supply primary. Do not attempt to service the power supply under these conditions. Disconnect the AC power cord prior to handling the power supply. When servicing any other system component, the AC power cord should remain connected and poses no safety hazard.

To install a replacement SBus card in the system unit:

1. **Remove the faulty SBus card.**
   Make sure you use the wrist strap and antistatic mat. Be sure to remember which slot contained the faulty SBus card.
2. **Read the manual supplied with the replacement SBus card.**
   Pay particular attention to the section describing the jumper or switch settings, slot requirements, and tools needed.
3. **Remove the replacement card from its antistatic bag. Hold the card by the edges.**
   Place the SBus card on an antistatic surface (either an antistatic mat or the antistatic bag the card was shipped in).
4. **If required, set the jumpers or switches on the card.**
   Refer to the manual supplied with the replacement SBus card.

5. **Replace the card.**
   Position the card in the same location that the faulty card occupied. Insert the two locating tabs on the card's mounting plate into the slots above the rectangular opening in the back panel.

Figure 6-7 Positioning an SBus Card



Connect the SBus card to its slot.

Align the connector on the card with the SBus slot on the main logic board. Press gently on the corners of the SBus card until the connection is secure. *Do not force the card.*

Caution – Do not press down on the SBus card retainer, as this can cause it to break. Using excessive force to secure the connection may bend or damage the connector pins.

6. **Refer to the manual supplied with the replacement card for instructions on any additional hardware setup.**
7. **Attach any internal cables leading from the SBus card to the main logic board (if applicable).**
8. **Attach any external cables that must be connected to the SBus card (if applicable).**
9. **Close enclosure (if any).**
10. **Turn on power.**

11. **Refer to the guide for your SBus product to complete any required software installation, configuration, or additional setup procedures.**

6.8 *Non-Volatile RAM (NVRAM)*

This section describes the removal and replacement procedures for the NVRAM chip. If you replace the main logic board, you must transfer the NVRAM chip from the faulty board to the replacement board.

Caution – The NVRAM chip is a delicate electronic component that is extremely sensitive to static electricity. Ordinary amounts of static from your clothes or work environment can destroy the NVRAM. Always wear a grounding strap when handling the NVRAM.

6.8.1 *Removing the NVRAM*

To remove the NVRAM:

1. **Prepare to work on the system.**
   Halt the system and verify that the power is off. Then open the enclosure (if any) and attach a wrist strap.

Caution – The AC power cord should remain attached between the system unit and an AC wall outlet. This connection provides the ground path necessary to protect internal system components from harmful static discharges. Inside the system unit, be sure the power supply wiring harness is connected to the main logic board to complete the ground.

Warning – Verify that the system power switch is in the Standby (⏻) position. The green LED at the front of the system unit should not be lit and the fan should not be running.

Warning – When the system power switch is in the Standby (⏻) position, and the AC power cord remains connected to a power outlet, hazardous AC voltage is still present in the power supply primary. Do not attempt to service the power supply under these conditions. Disconnect the AC power cord prior to handling the power supply. When servicing any other system component, the AC power cord should remain connected and poses no safety hazard.

2. **Locate NVRAM chip carrier on the main logic board.**

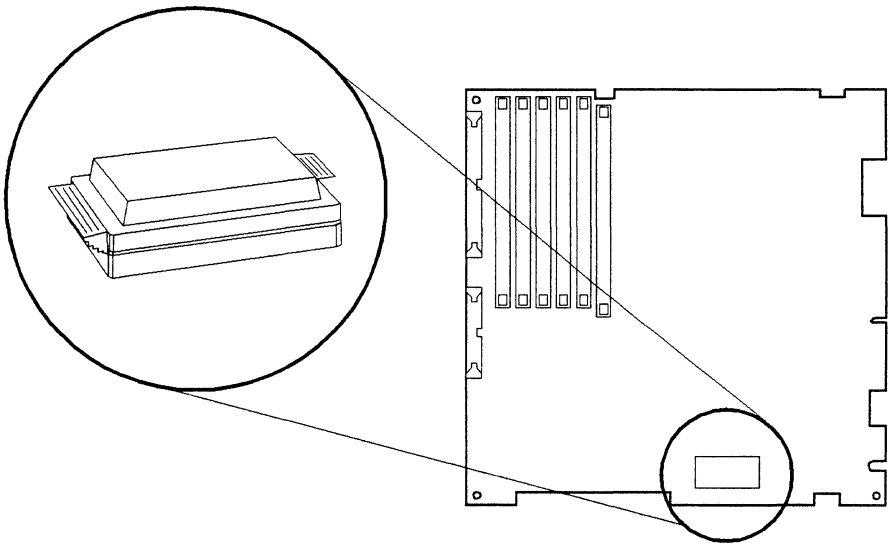
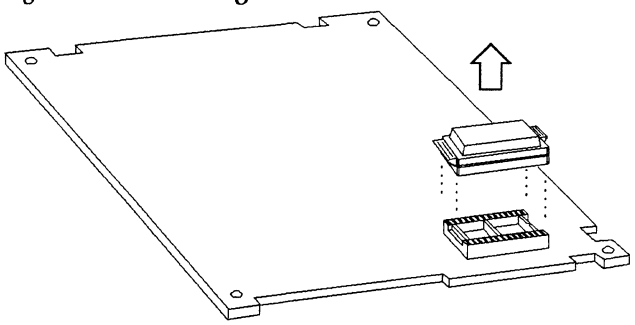


Figure 6-1 Locating the NVRAM

3. **Hold the NVRAM chip carrier on both ends and lift it straight up.** Gently wiggle the carrier as necessary.

Figure 6-9 Removing the NVRAM



4. **Place it on the antistatic mat.**

6.9.1 *Replacing the NVRAM*

To install the NVRAM on the main logic board:

1. **Hold the NVRAM chip on both sides of the carrier.**
2. **Carefully align the pins and insert the NVRAM chip into its socket.** The carrier is keyed so the NVRAM can be installed one way only.
3. **Push down on the NVRAM chip until it is fully seated in its socket.**
4. **Close the enclosure (if any).**
5. **Turn on power.**

6.10 Boot PROM

This section describes the removal and replacement procedures for the Boot PROM chip. If you replace the main logic board, you must transfer the Boot PROM chip from the faulty board to the replacement board.

Caution – The Boot PROM chip is a delicate electronic component that is extremely sensitive to static electricity. Ordinary amounts of static from your clothes or work environment can destroy the Boot PROM. Always wear a grounding strap when handling the Boot PROM.

6.10.1 Removing the Boot PROM

To remove the Boot PROM:

1. **Prepare to work on the system.**
   Halt the system and verify that the power is off. Then open the enclosure (if any) and attach a wrist strap.

Caution – The AC power cord should remain attached between the system unit and an AC wall outlet. This connection provides the ground path necessary to protect internal system components from harmful static discharges. Inside the system unit, be sure the power supply wiring harness is connected to the main logic board to complete the ground.

Warning – Verify that the system power switch is in the Standby (⏻) position. The green LED at the front of the system unit should not be lit and the fan should not be running.

Warning – When the system power switch is in the Standby (⏻) position, and the AC power cord remains connected to a power outlet, hazardous AC voltage is still present in the power supply primary. Do not attempt to service the power supply under these conditions. Disconnect the AC power cord prior to handling the power supply. When servicing any other system component, the AC power cord should remain connected and poses no safety hazard.

2. **Locate Boot PROM chip carrier on the main logic board.**
   See Figure 6-10.
3. **Hold the Boot PROM chip carrier on both ends and lift it straight up.**
   Gently wiggle the carrier as necessary (see Figure 6-11).
4. **Place it on the antistatic mat.**

Figure 6-10 Locating the Boot PROM

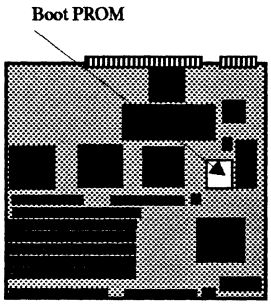
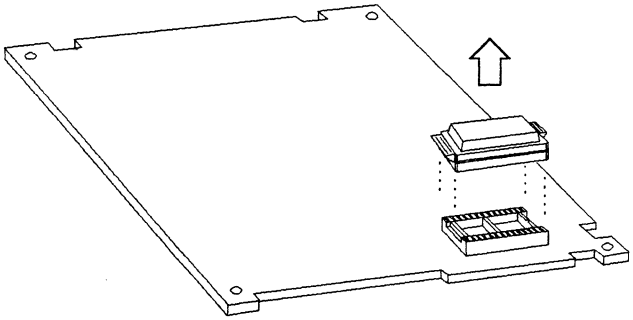


Figure 6-11 Removing the Boot PROM



Replacing the Boot PROM

To install the Boot PROM on the main logic board:

1. **Hold the Boot PROM chip on both sides of the carrier.**
2. **Carefully align the pins and insert the Boot PROM chip into its socket.** The carrier is keyed so the Boot PROM can be installed one way only.
3. **Push down on the Boot PROM chip until it is fully seated in its socket.**
4. **Close the enclosure (if any).**
5. **Turn on power.**

6.12 *Turning On the Power*

Warning – Before powering on your system, be sure to close the system unit. It is not safe to operate your SPARCstation while the system unit is open.

Warning – This device must be equipped with a 3-wire grounded power cord. To reduce the risk of electrical shock, always plug the power cord into a properly grounded power outlet.

Caution – Always allow 10 seconds between turning off the power and turning it back on again. This pause prevents possible damage to power supply components in your system unit.

After turning off the power to replace a part, turning the power back on again is relatively simple:

1. **Turn on the power in this sequence:**
   a. External drive units (if any), starting with the unit that is furthest electrically from the system unit
   b. Monitor (if you turned it off)
   c. Desktop SPARCstation system unit
2. **Boot the operating system.**
   The operating system may start to boot automatically, or you may need to enter a command at the system prompt. What you do next depends on the operating system software you are using. Consult the documentation supplied with your operating system for instructions on booting and logging in to your system.

SPARCclassic Engine Address Space

7.1 Required Reference Materials

Reference material required for a complete definition of the SPARCclassic Engine:

The SPARC Architecture Manual, Sun Part No. 800-1399-xx.

microSPARC Data Sheet, Texas Instruments, August, 1992. (Appendix L)

microSPARC Reference Guide, Texas Instruments, January, 1993. (Appendix K)

NCR SBus I/O Chipset Data Manual, NCR Corporation, February, 1993. (Appendix M)

7.2 The Address Space Indicator (ASI) Spaces

At the CPU, all addresses are virtual addresses, augmented with the Address Space Identifier (ASI) bits used in CPU instructions. Each ASI may be thought of as an extension to the virtual address. A single ASI represents 4 GB of addressable space.

ASIs are defined with eight bits. Eight bits create an ideal two hundred and fifty-six 4 GB address areas. (The eight ASI bits are part of the SPARC architecture, and are described in the *SPARC Architecture Manual*.)

The SPARCclassic Engine CPU uses 15 ASI address spaces, thereby allowing (in theory) for fifteen 4 GB addressable spaces.

The fifteen ASIs are sub-divided into two broad categories: virtual space and physical space. Virtual space contains control devices for the CPU, Main Memory Cache and the MMU itself; physical space contains physical address devices accessed through the MMU.

The SPARCclassic Engine ASI categories are defined in the following table:

Table 7-1 The Address Space Indicator (ASI) Categories

Type of Space	ASI Hex	ASI Value	Type of Space
Control Space	ASI 0x3	03	Reference MMU Flush/ Probe
	ASI 0x4	04	CPU Module Control Space
	ASI 0x6	06	Reference MMU Diagnostics
	ASI 0xC	12	Instruction Cache Tag
	ASI 0xD	13	Instruction Cache Data
	ASI 0xE	14	Data Cache Tag
	ASI 0xF	15	Data Cache Data
	ASI 36	54	Instruction Cache Flash Clear
	ASI 37	55	Data Cache Flash Clear
	ASI 39	57	Data Cache Diagnostic Access
Physical Space	ASI 0x8	08	User Instruction
	ASI 0x9	09	Supervisor Instruction
	ASI 0xA	10	User Data
	ASI 0xB	11	User Instruction
	ASI 20	32	MMU Bypass

The SPARCclassic Engine CPU automatically sets the ASI bits correctly for accesses to physical space (user data, user instruction, supervisor data, and supervisor instruction). To access virtual space, use the alternate space instructions described in the *SPARC Architecture Manual* to force the ASI bits to the desired value.

The following graphic representations of the SPARCclassic Engine's address spaces are intended to best display the organization of the virtual and physical memory space.

7.3 *The SPARCclassic Engine Memory Maps*

Below is a table of the SPARCclassic Engine Address Space Identifier (ASI) space. The address space (ideal) for each ASI is 4 GB (0x0000 0000 to 0xFFFF FFFF).

Table 7-1 Address Space Identifiers Used by microSPARC

ASI	Definition	Access	Size	Comments
0	Reserved	--	--	Virtual Space
1	Unassigned	--	--	Virtual Space
2	Unassigned	--	--	Virtual Space
3	Reference MMU Flush/Probe	Read/Write	Single	Virtual Space
4	CPU Module Control Space	Read/Write	Single	Virtual Space
5	Unassigned	--	--	Virtual Space
6	Reference MMU Diagnostics	Read/Write	Single	Virtual Space
7	Unassigned	--	--	Virtual Space
8	User Instruction	Read/Write	All	Physical Space
9	Supervisor Instruction	Read/Write	All	Physical Space
0A	User Data	Read/Write	All	Physical Space
0B	Supervisor Data	Read/Write	All	Physical Space
0C	Instruction Cache Tag	Read/Write	Single	Virtual Space
0D	Instruction Cache Data	Read/Write	Single	Virtual Space
0E	Data Cache Tag	Read/Write	Single	Virtual Space
0F	Data Cache Data	Read/Write	Single	Virtual Space
10	Unassigned	--	--	Virtual Space
11	Unassigned	--	--	Virtual Space
12	Unassigned	--	--	Virtual Space
13	Unassigned	--	--	Virtual Space

Table 7-1 Address Space Identifiers Used by microSPARC

ASI	Definition	Access	Size	Comments
14	Unassigned	--	--	Virtual Space
15	Reserved	--	--	Virtual Space
16	Reserved	--	--	Virtual Space
17	Unassigned	--	--	Virtual Space
18	Unassigned	--	--	Virtual Space
19	Unassigned	--	--	Virtual Space
1A	Unassigned	--	--	Virtual Space
1B	Unassigned	--	--	Virtual Space
1C	Unassigned	--	--	Virtual Space
1D	Reserved	--	--	Virtual Space
1E	Reserved	--	--	Virtual Space
1F	Unassigned	--	--	Virtual Space
20	Reference MMU Bypass	Read/Write	All	Physical Space
21	Reserved	--	--	Virtual Space
22	Reserved	--	--	Virtual Space
23	Reserved	--	--	Virtual Space
24	Reserved	--	--	Virtual Space
25	Reserved	--	--	Virtual Space
26	Reserved	--	--	Virtual Space
27	Reserved	--	--	Virtual Space
28	Reserved	--	--	Virtual Space
29	Reserved	--	--	Virtual Space
2A	Reserved	--	--	Virtual Space
2B	Reserved	--	--	Virtual Space
2C	Reserved	--	--	Virtual Space
2D	Reserved	--	--	Virtual Space
2E	Reserved	--	--	Virtual Space

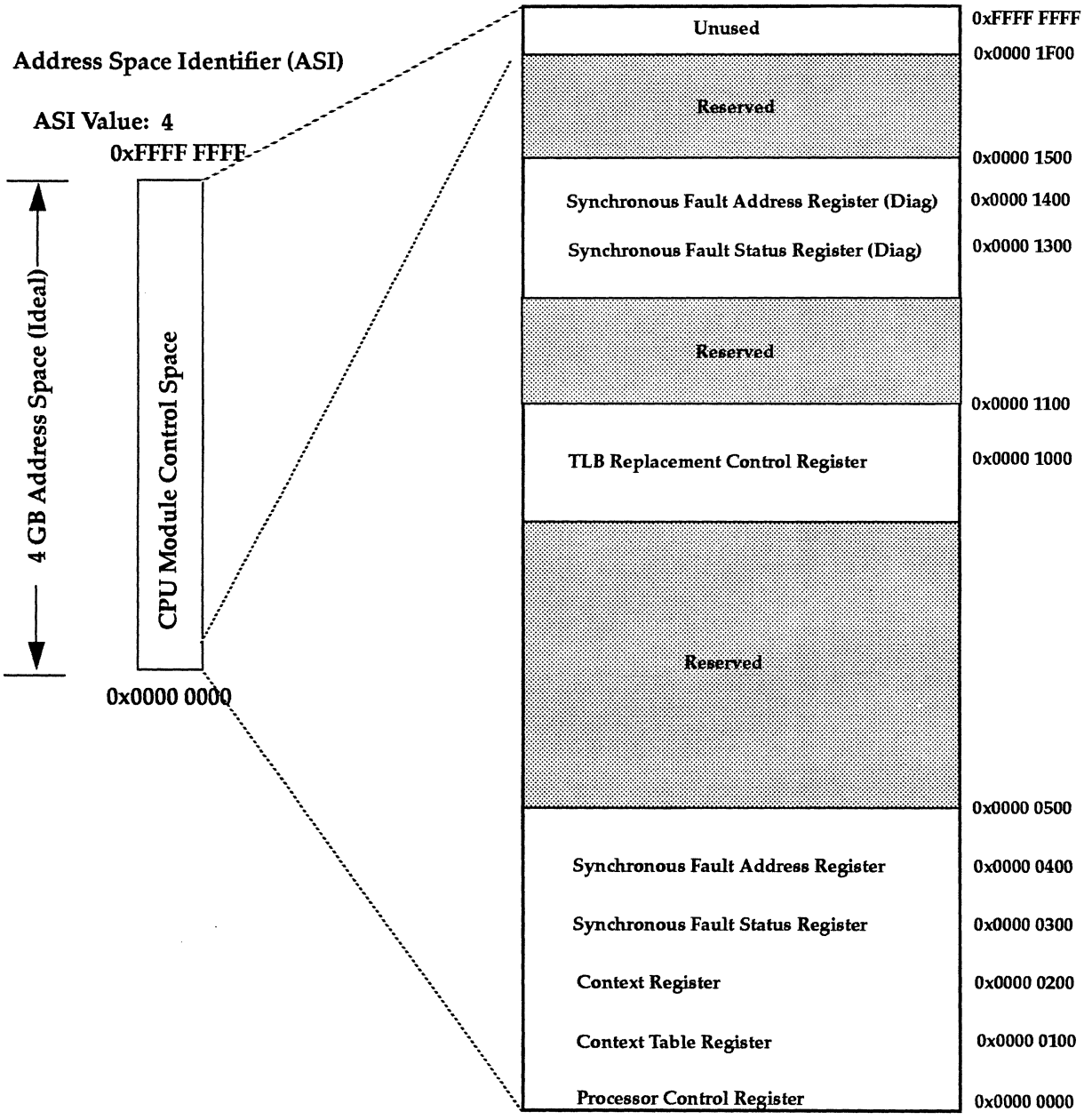
Table 7-1 Address Space Identifiers Used by microSPARC

ASI	Definition	Access	Size	Comments
2F	Reserved	--	--	Virtual Space
30	Unassigned	--	--	Virtual Space
31	Unassigned	--	--	Virtual Space
32	Unassigned	--	--	Virtual Space
33	Unassigned	--	--	Virtual Space
34	Unassigned	--	--	Virtual Space
35	Unassigned	--	--	Virtual Space
36	Instruction Cache Flash Clear	Write	Single	Virtual Space
37	Data Cache Flash Clear	Write	Single	Virtual Space
38	Unassigned	--	--	Virtual Space
39	Data Cache Diagnostic Access	Read/Write	Single	Virtual Space
3A	Unassigned	--	--	Virtual Space
3B	Unassigned	--	--	Virtual Space
3C	Unassigned	--	--	Virtual Space
3D	Unassigned	--	--	Virtual Space
3E	Unassigned	--	--	Virtual Space
3F	Unassigned	--	--	Virtual Space
40-FF	Reserved	--	--	Virtual Space

Address Space Identifier 4 represents the CPU Module Control Space. Within this ideal 4 GB of virtual memory resides the MMU Registers. Figure 6-1 on the next page displays the ASI 4 contents graphically.

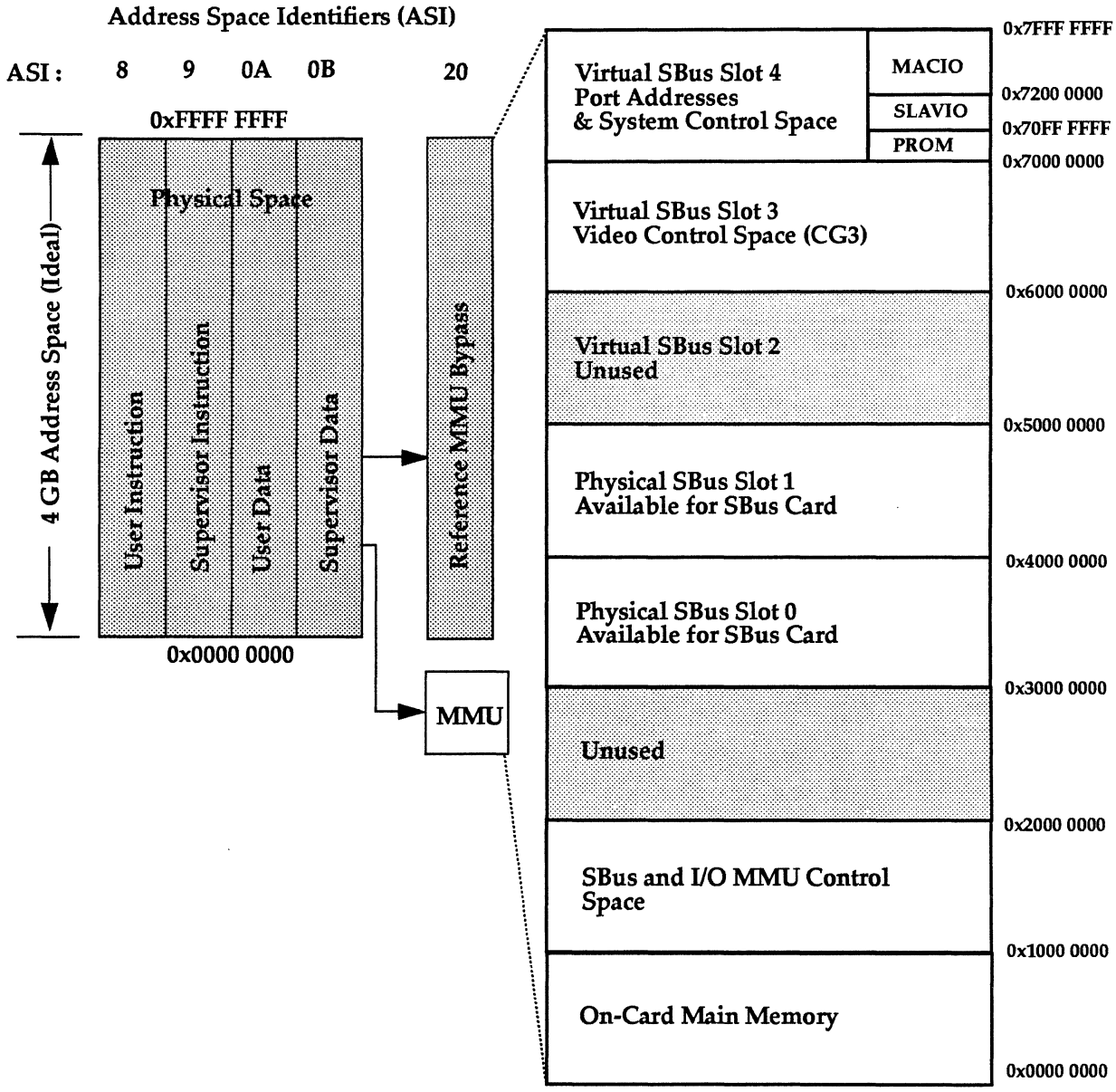
NOTE: All graphic representations of memory space presented in this chapter are not in proportion; the graphic elements intend to give only the roughest indication of memory size.

Figure 6-1 Virtual Memory Map: CPU Module Control Space



Physical address space is represented in five ASIs. Figure 6-2 below graphically represents the five physical address space ASIs, and shows how the virtual address space is transformed by/bypassed by the MMU into the physical address space.

Figure 6-2 Virtual to Physical (MMU) Memory Map: Physical Address Space



SBus Slot #4 is further divided into Boot PROM address space, system control space (SLAVIO) and port address space (MACIO). Figures 6-3 and 6-4 graphically represent the SBus Slot #4 address space.

Figure 6-3 Physical Memory Map: SBus Slot 4 SLAVIO System Control Space

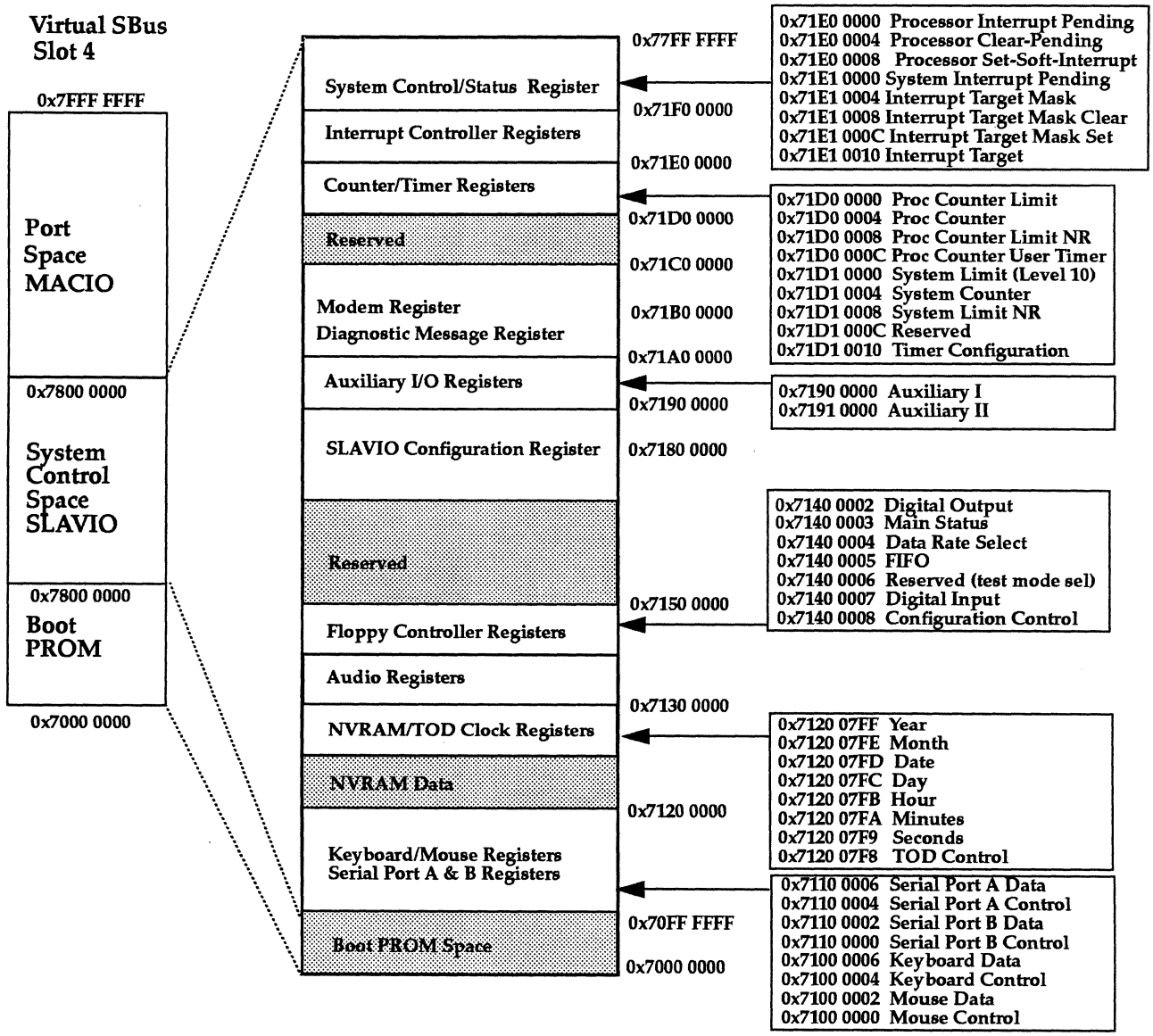
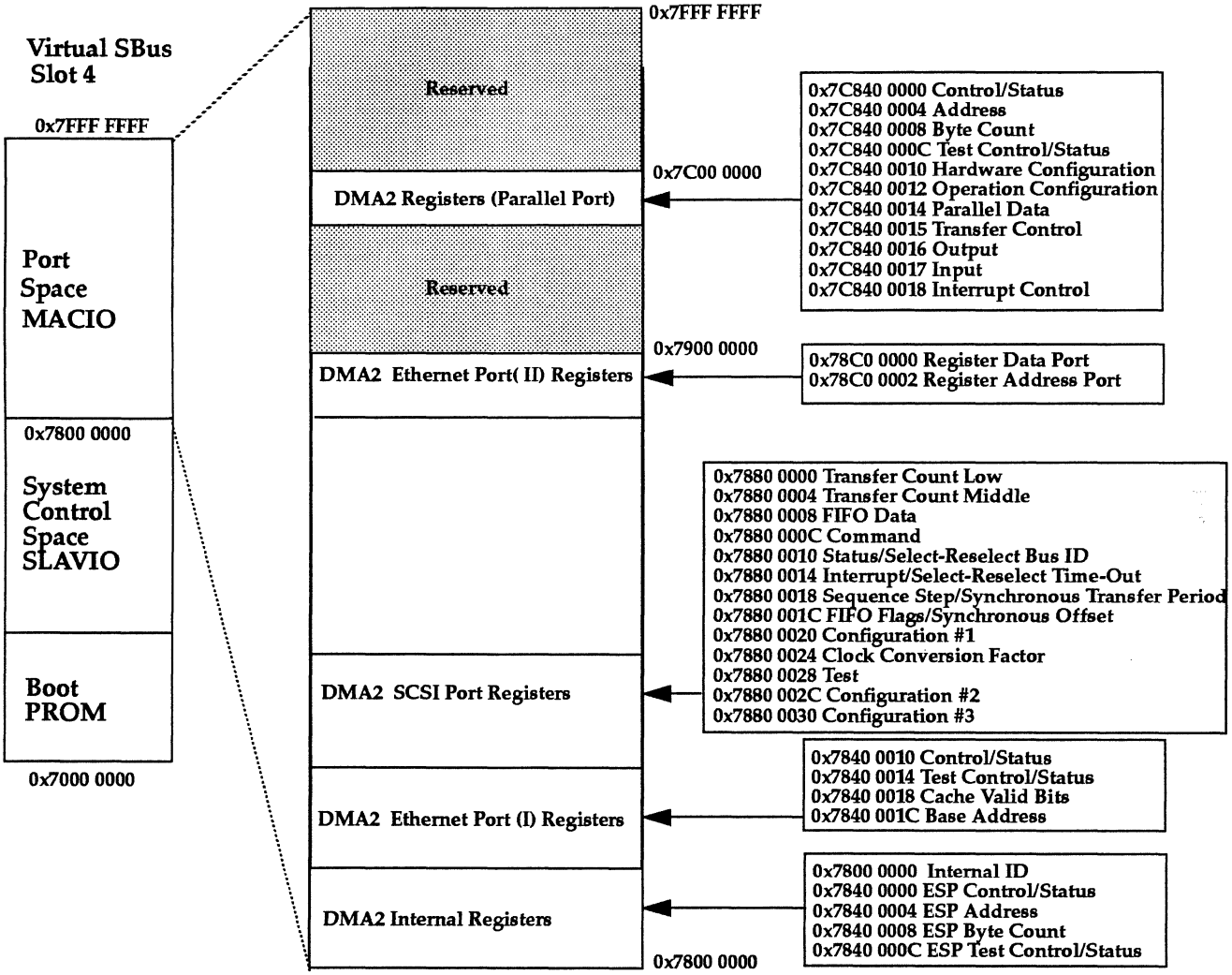


Figure 6-4 Physical Memory Map: SBus Slot 4 MACIO Port Space



7.4 *The SBus Address Bus Cycles*

The SPARCclassic Engine supports two different address SBus cycles, a virtual address bus cycle and the physical address bus cycle.

7.4.1 *The Virtual Address SBus Cycles*

The CPU (IU, FPU and cache) operates with virtual addresses only, and communicates directly with the MMU with virtual addresses. All control space registers are accessed with virtual addresses on the SBus.

7.4.2 *The Physical Address SBus Cycles*

If there is a 'cache miss,' the cache accesses the MMU with a virtual address. The MMU translates all virtual addresses into physical addresses to access main memory and all I/O devices on the SBus. SPARCclassic Engine board devices in physical space are accessed with physical addresses (virtual addresses translated by the MMU) on the SBus.

7.5 *Timeout Errors*

Accesses to non-existent devices on CPU bus cycles to microSPARC control space or device space will cause timeout errors.

During system space accesses, timeout errors result from accesses to invalid codes within defined fields, or from accesses to un-implemented system space devices, where A[31:28] are not legal values.

In device space, timeout errors result from accesses to addresses outside the defined address space, or accesses to I/O devices which are legal but not present.

7.6 *Error Registers*

The SPARCclassic Engine provides two types of error registers. They are:

- The **bus error registers** are in microSPARC control space. After a memory error exception, these registers identify the cause and location of the error.
- The **main memory error registers (on-card)** are in device space.

Open Boot PROM

8.1 Required Reference Materials

Reference material required for a complete definition of the SBus:

Introduction to Open Boot 2.0,
Sun Part No. 800-5674-10

Open Boot 2.0 Command Reference,
Sun Part No. 800-6076-10

Open Boot 2.0 Command Summary,
Sun Part No. 800-5675-10

Writing FCode Drivers for SBus Cards,
Sun Part No. 800-5673-10

SBus Developer's Kit II+,
Sun Part No. 605-1307-xx.

8.2 SPARCclassic Engine Open Boot PROM (Version 2.0)

The SPARCclassic Engine has Version 2.0 of the Sun Microsystems Open Boot PROM.

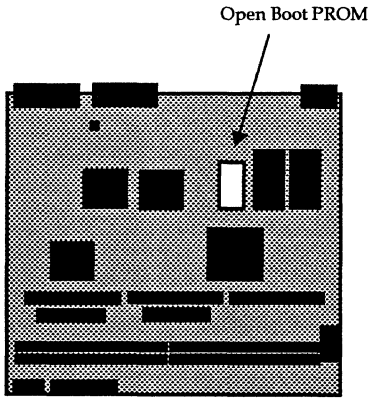
There is one Boot PROM socket on SPARCclassic Engine, providing up to 2 MB of read-only memory (ROM), containing the boot code, FORTH code, and on-card diagnostics code.

Within the *SBus Developer's Kit*, there is a book entitled *Open Boot PROM 2.0 Toolkit User's Guide*. This book includes the information about the 2.0 Open Boot PROM for the SPARCclassic Engine. Use this book to define the functionality and operation of the 2.0 version of the boot PROM.

The Open Boot PROM is the SPARCclassic Engine start-up device and all other components on the card relate to the Open Boot PROM. Substantial information is available in the *Open Boot PROM 2.0 Toolkit User's Guide*, and much of it is required for understanding the *SPARCclassic Engine OEM Technical Manual*. Be sure to order the *SBus Developer's Kit*, if you have not already done so.

8.3 *Location of the Open Boot PROM*

Figure 7-1 Location of the Open Boot PROM



Diagnostics

9.1 Required Reference Materials

Reference material required for a complete definition of the SPARCclassic Engine on-card diagnostics:

Sundiag User's Guide, Sun Microsystems, Inc., 1992.
Sun Part No. 800-2841-xx

SunDiagnostic Executive User's Guide for SPARCstations, Sun Microsystems, Inc.,
Sun Part No. 800-2326-xx

Introduction to Open Boot 2.0, Sun Microsystems, Inc., 1992.
Sun Part No. 800-5674-10

Open Boot 2.0 Command Reference, Sun Microsystems, Inc., 1992.
Sun Part No. 800-6076-10

Open Boot 2.0 Command Summary, Sun Microsystems, Inc., 1992.
Sun Part No. 800-5675-10

Writing FCode Drivers for SBus Cards, Sun Microsystems, Inc., 1992.
Sun Part No. 800-5673-10

SBus Developer's Kit II+, Sun Microsystems, Inc., 1991,
Sun Part No. 605-1307-xx

Sunergy PROM Based Diagnostics for Bring-up, Sun Microsystems, Inc., 1991,

9.2 *Introduction to SPARCclassic Engine Diagnostics*

This section describes the different types of diagnostic firmware and software tools available to you and how they are related. The main categories of diagnostics are:

- Boot PROM diagnostics
  - Power-On Self-Test (POST)
  - On-Board Diagnostics
- Sundiag System Exerciser
- SunDiagnostic Executive
- Forth Toolkit

The text in this chapter is written at the "system" level, because you need to have a keyboard and some type of monitor/printer to view the results of the tests. The specifics of the procedures that follow must be adjusted to your particular situation.

Normally, you will require a terminal connected to the SPARCclassic Engine serial port. If you are using alternate equipment, read and understand the documentation that is provided with that equipment, and adjust the following procedures accordingly.

The flowchart below outlines the roles played by various diagnostics during the default boot mode.

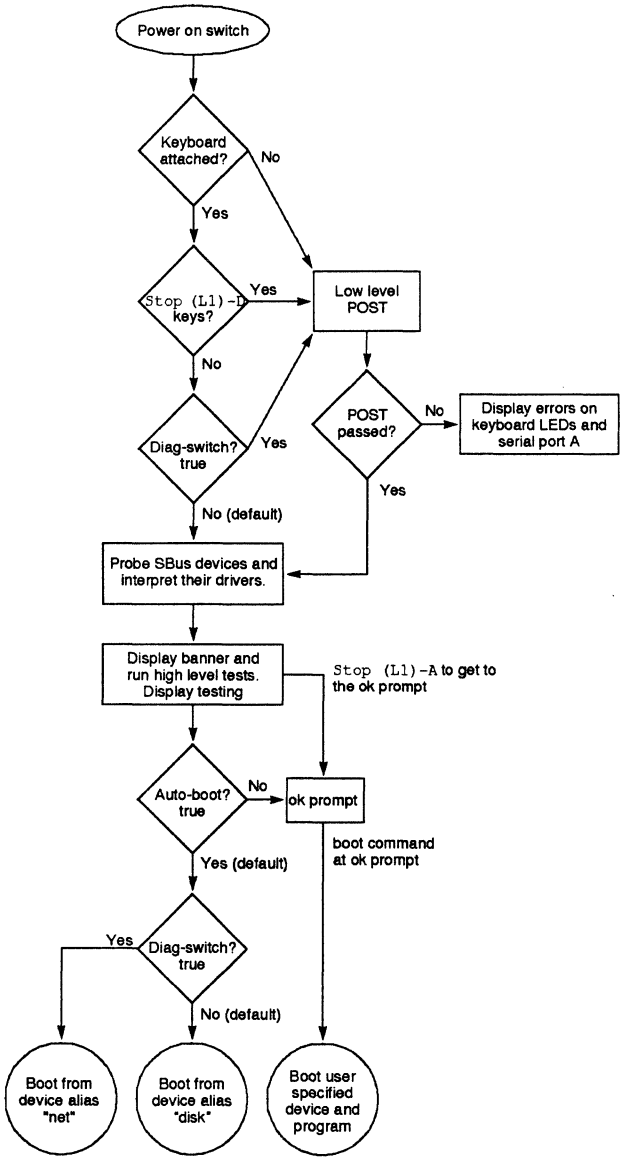


Figure 9-1 Default Boot Mode

9.2 *How It Fits Together*

This section describes how the various diagnostic tools work together in the different power-on modes. This description assumes you are using a graphics monitor to view test results.

POST will run automatically at power on, if the **Stop (L1) - D** keys are pressed or the `diag-switch?` parameter is set true.

If the POST passes, the system probes for SBus devices and interprets their drivers. Next, high level tests are performed. You will see the word `Testing` while the high level tests are running. After `Testing` is displayed, if you want to enter the Forth Toolkit, (indicated by the `ok` prompt), press the **Stop (L1)-A** keys simultaneously.

If the autoboot switch parameter is set to false (not the default), you will obtain the `ok` prompt. The ok prompt is the default prompt. To change to the Monitor prompt (>) see the *Introduction to Open Boot 2.0*.

If the autoboot switch parameter is set to true (default), and the diagnostic switch parameter is set to false (default), Solaris is booted using the device alias "disk". If the autoboot switch parameter is set to true (default), and the diagnostic switch parameter is set to true (not the default), Solaris is booted using the device alias "net".

To boot user-specified programs, such as the SunDiagnostic Executive, you must be at the `ok` prompt. See "On-Board Diagnostics" later in this chapter for a detailed procedure on how to obtain the `ok` prompt.

Table 9-1 Autoboot and Diagnostic Switch Parameter

Autoboot Switch Parameter	Diagnostic Switch Parameter	Results
False	(Don't care)	ok prompt (Forth Toolkit)
True	False	Boot Solaris (vmunix) from disk
True	True	Boot Solaris (vmunix) from net

9.2 *When to Use Diagnostics*

You should use each type of diagnostic tool in the appropriate circumstances. Table 9-2 provides a summary of the available diagnostic tools and lists when to use each diagnostic tool.

Table 9-2 Summary of Available Diagnostic Tools

Diagnostic Tool	When or why to use
Power-On Self Test	Executes at power-on when **Stop (L1)-D** keys are pressed or the `diag-switch?` parameter is set true. The POST code resides in the Boot PROM and is driven by the Pok (Power ok) signal from the power supply. POST tells you if the SPARCclassic Engine, the DSIMM in slot 1. Described later in this chapter.
On-Board Diagnostics	Tests such as the Ethernet test. You must be at the `ok` prompt to run on-board diagnostics. The On-Board diagnostics reside in the Boot PROM. Described later in this chapter.
Sundiag System Exerciser	Runs under Solaris. It displays real-time use of the system resources and peripherals. The Sundiag System Exerciser tells you if your system is functioning correctly or not. If Sundiag fails, run the Power-On Self-Test. If all power-on self-tests pass, then run the SunDiagnostic Executive to identify the problem. See the *Sundiag User's Guide* for more information.
SunDiagnostic Executive	Runs extensive, configurable subsystem tests independent of Solaris. Run the SunDiagnostic Executive if all tests pass when you run POST. Running the SunDiagnostic Executive allows you to troubleshoot which field replaceable unit needs to be replaced. See the latest version of *SunDiagnostic Executive User's Guide for the SPARCstations* for more information.
Forth Toolkit	Allows input to the system at the Boot PROM level. Supports functions such as changing NVRAM parameters, resetting the system, running diagnostic tests, displaying system information, and redirecting input and output. See the *Open Boot PROM 2.0 Toolkit User's Guide* for more information.

9.3 *Boot PROM Diagnostics*

The diagnostics stored in the Boot PROM include the following:

- Power-On Self-Test
- On-Board Diagnostics

If there is system trouble, you may want to run extended on-board diagnostics to take advantage of thorough tests including — but not limited to — Ethernet and memory tests.

The Boot PROM diagnostics are described in the following sections.

9.3.1 *Power-On Self Test (POST)*

The Power-On Self-Test (POST) runs when you turn on the system power switch and one of the following conditions apply:

- Press **`Stop (L1)-D`** keys
- The `diag-switch?` NVRAM parameter is set true
- The system keyboard is disconnected

The POST code, which resides in the Boot PROM, is executed by the CPU (IU) when the Pok signal is received from the power supply. The POST consists of a sequence of tests designed to test the major hardware components of the SPARCclassic Engine before attempting to boot Solaris. POST does not perform extensive testing on any component of the SPARCclassic Engine. Only major failures can be detected by POST.

If a failure occurs in POST, it simply stops. Because there is no keyboard port to support a Sun-5 keyboard that displays LED diagnostic patterns, there is no methodology to know why the POST failed without watching the test as it progresses.

Following the system successful initialization, SunOS is booted automatically, unless the NVRAM configuration options specify not to do so.

9.3.2 *Power-On Self Test Detailed Description*

This section describes the keyboard LED state that results from POST and gives its meaning.

If all POST tests pass, run the SunDiagnostic Executive with the cache disabled. The SunDiagnostic Executive is an independent operating system. It runs exhaustive subsystem tests independent of Solaris. See the latest version of *SunDiagnostic Executive User's Guide for the SPARCstations*.

9.3.3 *On-Board Diagnostics*

You have access to a number of tests called On-board diagnostics. To invoke these tests, you must enter the Forth Toolkit.

Caution – In order to run On-board diagnostics, you must halt the system in an orderly manner. When the operating system or any other stand-alone program has already booted, do not use the **Stop (L1)-A** keys to halt the system. Abruptly aborting program execution may cause damage to data files.

To run On-board diagnostics:

1. **Save all your work and quit all applications.**
2. **As `root`, halt the system by entering** `/usr/sbin/halt`.
   You are presented with the `ok` prompt. The `ok` prompt is the default prompt. If you want to change the default prompt to the `>` prompt, see the *Introduction to Open Boot 2.0*.
3. **Enter** `help diag` **to get a listing of tests comprising on-board diagnostics.**

Figure 9-2 summarizes the steps you need to take to halt the system, enter the Forth Toolkit, and list the diagnostic tests.

```
hostname#    /usr/sbin/halt
ok help diag
     Category:  Diag (diagnostic routines)
test   device-specifier ( -- ) run selftest method for specified device
     Examples:
         test /iommu/sbus/ledma@f,400010/le   - test net
         test net           - test net  (device-specifier is an alias)
         test scsi          - test scsi (device-specifier is an alias)
         test floppy        - test floppy disk drive
watch-clock          (--)   - show ticks of real-time clock
watch-net            (--)   - monitor broadcast packets using auto-selected interface
watch-aui            (--)   - monitor broadcast packets using AUI interface
watch-tpe            (--)   - monitor broadcast packets using TPE interface
watch-net-all        (--)   - monitor broadcast packets on all net interfaces
probe-scsi           (--)   - show attached SCSI devices
probe-scsi-all       (--)   - show attached SCSI devices for all host adapters
test-all             (--)   - execute test for all devices with selftest method
test-memory         (--)   - test all memory if diag-switch? is true, otherwise test memory
                              specified by selftest-#megs
```

Figure 9-2 Halting the System and Displaying On-Board Diagnostics

These on-board tests allow you to test the network controller, the diskette drive system, memory, and the system clock.

Test <alias name>, Test <device path>

The `test` command, combined with a device alias or device pathname, will execute that device selftest program. If a device has no selftest program, this message will be displayed: `No selftest method for <device name>`. To run the selftest program for a device, type the `test` command followed by the device alias or device pathname. For example:

```
ok test floppy
Testing floppy disk system.  A formatted disk should be in the drive.
Test succeeded.
```

The following tests are supported in the SPARCengine EC system.

Type of Tests	Description
`test screen`	Tests the system video graphics hardware and monitor. The `diag-switch?` NVRAM parameter must be set true for the test to run.
`test floppy`	Tests the floppy drive ability to respond to commands. Requires a formatted diskette to be inserted into the drive.
`test scsi`	Tests the SCSI interface logic on the SPARCclassic Engine. The `diag-switch?` NVRAM parameter must be set true for the test to run.
`test net-aui`	Performs an internal and external loopback test on the AUI (Thick) Ethernet interface. A cable must be connected to the system AUI Ethernet port and to an Ethernet Tap or the test will fail the external loopback phase.
`test net-tpe`	Performs an internal and external loopback test on the TPE interface. A cable must be connected to the system TPE port and to a TPE hub or the test will fail the external loopback phase. If the `tpe-link-test?` parameter is false (disabled), the external loopback test will appear to pass even if a cable is not connected.
`test net`	Performs an internal and external loopback test on the auto-selected system Ethernet interface. A cable must be attached to the system and to an Ethernet tap or hub or the external loopback test will fail.

`test disk`
`test disk0`
`test disk1`
`test disk2`
`test disk3`
	Tests internal or external SCSI disks which have a self diagnostic program contained in the drive controller. The drive must be spinning before this test is executed or the test will fail. Enter a `boot <disk alias>` command to cause the drive to spin up. (`disk` and `disk0` = SCSI target 3, `disk1` = SCSI target 1, `disk2` = SCSI target 2, `disk3` = SCSI target 0.)

`test cdrom`	Performs a selftest diagnostic on the CDROM drive. The CDROM must be set to SCSI target 6 and have a CD inserted or the test will fail.

`test tape`
`test tape0`
`test tape1`
	Tests the SCSI tape drive by executing the drive selftest program. (`tape` and `tape0` = SCSI target 4, `tape 1` = SCSI target 5).

`test ttya`	This test outputs an alphanumeric test pattern on the system serial port (`ttya` = serial port). You must attach a terminal to the tested port to observe the output.
`test keyboard`	This test executes the keyboard selftest. The four LEDs on the keyboard should flash on once, and this message is displayed: `Keyboard Present.`

Test-all

The `test-all` command tests all devices in the system which have a selftest program. Tests are executed in order using the device tree (viewed with the `show-devs` command) as reference. Disks, tapes, and CDROMs are not tested by `test-all`.

Watch-clock

This test reads a register in the NVRAM/TOD (Non-Volatile RAM/Time of Day) chip on the SPARCclassic Engine and displays the result as a seconds counter. The counter should count from 0 to 59 repeatedly until you interrupt it by pressing any key on the keyboard.

The following screen gives you an example of a `watch-clock` test.

```
ok watch-clock
Watching the 'seconds' register of the real time clock chip.
It should be 'ticking' once a second.
Type any key to stop
41
```

Watch-net, Watch-aui, Watch-tpe and Watch-net-all

These tests monitor broadcast Ethernet packets on the Ethernet cable(s) connected to the system. Good packets received by the system are indicated by a period (`.`) displayed on the screen. Errors are indicated with an `X` and the error description. See the following example:

```
ok watch-net
 Internal loopback test -- succeeded.
 External loopback test -- Auto-selecting Ethernet cable I/F
Trying AUI
Received packet on AUI
Select cable - AUI
succeeded.
Looking for Ethernet packets.
'.' is a good packet.  "X" is a bad packet.
Type any key to stop.
.....................................................................
.....................................................................
..................Framing error CRC error X..................
```

Probe-scsi, Probe-scsi-all

The `probe-scsi` test sends an inquiry command to internal and external SCSI devices connected to the SPARCengine EC on-board SCSI interface. If a SCSI device is connected and powered up, the target address, unit number, device type, and manufacturer name should be displayed. For example:

```
ok probe-scsi
Target 3
  Unit 0 Disk SEAGATE ST1480 SUN04245828 Copyright (c) 1991 Seagate All rights reserved.
```

The `probe-scsi-all` test sends an inquiry command to all SCSI devices on all the SCSI host adapters installed in the system. The first identifier listed in the display is the SCSI host adapter address in the system device tree, followed by the SCSI device identification data. For example:

```
ok probe-scsi-all
/iommu@f,e0000000/sbus@f,e0001000/dma@1,81000/esp@1,80000
Target 2
  Unit 0 Disk SEAGATE ST41600N SUN1.3G00286965 Copyright (c)1991 Seagate All rights reserved.

/iommu@f,e0000000/sbus@f,e0001000/espdma@f,400000/esp@f,800000
Target 3
  Unit 0 Disk SEAGATE ST1480 SUN04245828 Copyright (c)1991 Seagate All rights reserved.
```

Test-memory

All of the system main memory will be tested if the system `diag-switch?` parameter is true. If the `diag-switch?` parameter is false, this test uses the `selftest-#megs` parameter in NVRAM to determine how much memory to test. The default for the `selftest-#megs` parameter is 1, so only 1 MB of memory is tested.

To change the amount of memory tested using the `selftest-#megs` parameter, type this command:

```
ok setenv selftest-#megs 16
```

This sets the desired memory size to 16 MB. Any whole number may be used as long as it does not exceed the actual size of memory (in MB) installed in the system. When the `test-memory` diagnostic is running, the number of MB being tested is displayed and counted down to zero during the test.

9.3 *Sundiag System Exerciser*

Use the Sundiag System Exerciser, which runs under Solaris, to determine real-time use of system resources and peripheral equipment such as SCSI devices. The Sundiag System Exerciser verifies that the system is functioning properly.

The exerciser is shipped with Solaris. If it has been selected during the SunInstall (operating system loading) procedure, it can be run at any time and is found in the directory `/usr/diag/sundiag`. If the Sundiag System Exerciser is not found on the system hard disk or server, you can load it from CD.

For information on how to use the Sundiag System Exerciser, see the *Sundiag User's Guide*. Appendix A, "Loopback Connectors," in the *Sundiag User's Guide* explains how to connect the external loopback connectors required for some options.

NOTE: Sundiag requires a configuration that includes a SPARCclassic Engine Ethernet daughter card. When Sundiag probes the SPARCclassic Engine, it accesses the NCR89C100 and finds an Ethernet controller, assumes that there is a net connection, and probes the net. If there is no Ethernet daughter card, Sundiag will not come up, responding with "probing routine failed."

If Sundiag passes, the system is operating properly. If Sundiag fails, the error messages should indicate the part of the system which has failed. If the error messages are not descriptive enough, you may need to run POST or the Sun Diagnostic Executive.

9.4 *SunDiagnostic Executive*

The SunDiagnostic Executive is an independent operating system. It runs exhaustive subsystem tests independent of Solaris. Run the SunDiagnostic Executive if all POST tests pass in order to determine which field-replaceable unit needs to be replaced. For information on POST, see "Power-On Self-Test Detailed Description" earlier in this chapter. The SunDiagnostic Executive, which provides you with thorough diagnostics, is described in the *SunDiagnostic Executive User's Guide for the SPARCstations.*

9.5 *Forth Toolkit*

The Forth Toolkit is a basic diagnostic utility and system interface. If there is any problem with your operating system, the Forth Toolkit automatically starts, indicated by the `ok` prompt. You can also choose to enter the Forth ToolKit by halting the system.

To enter the Forth Toolkit:

1. **Save all your work and quit all applications.**
   The following screen summarizes the steps you need to take to halt the system and enter the Forth Toolkit.

```
hostname#  /usr/etc/halt
syncing file systems .... done
Halted

ok
```

2. **As `root`, enter** `/usr/etc/halt`.
   The system syncs the file systems and brings you to the `ok` prompt.
3. **The system automatically enters the Forth Toolkit.**
   The `ok` prompt shows that you are in the Forth Toolkit.

For extensive information on tests you can run from the Forth Toolkit see *Introduction to Open Boot 2.0.*

SPARCclassic Engine Drawings

A.1 SPARCclassic Engine Mechanical Drawings

On the next few pages are the SPARClassic Engine mechanical drawings. Use the drawings to determine the product size and shape.

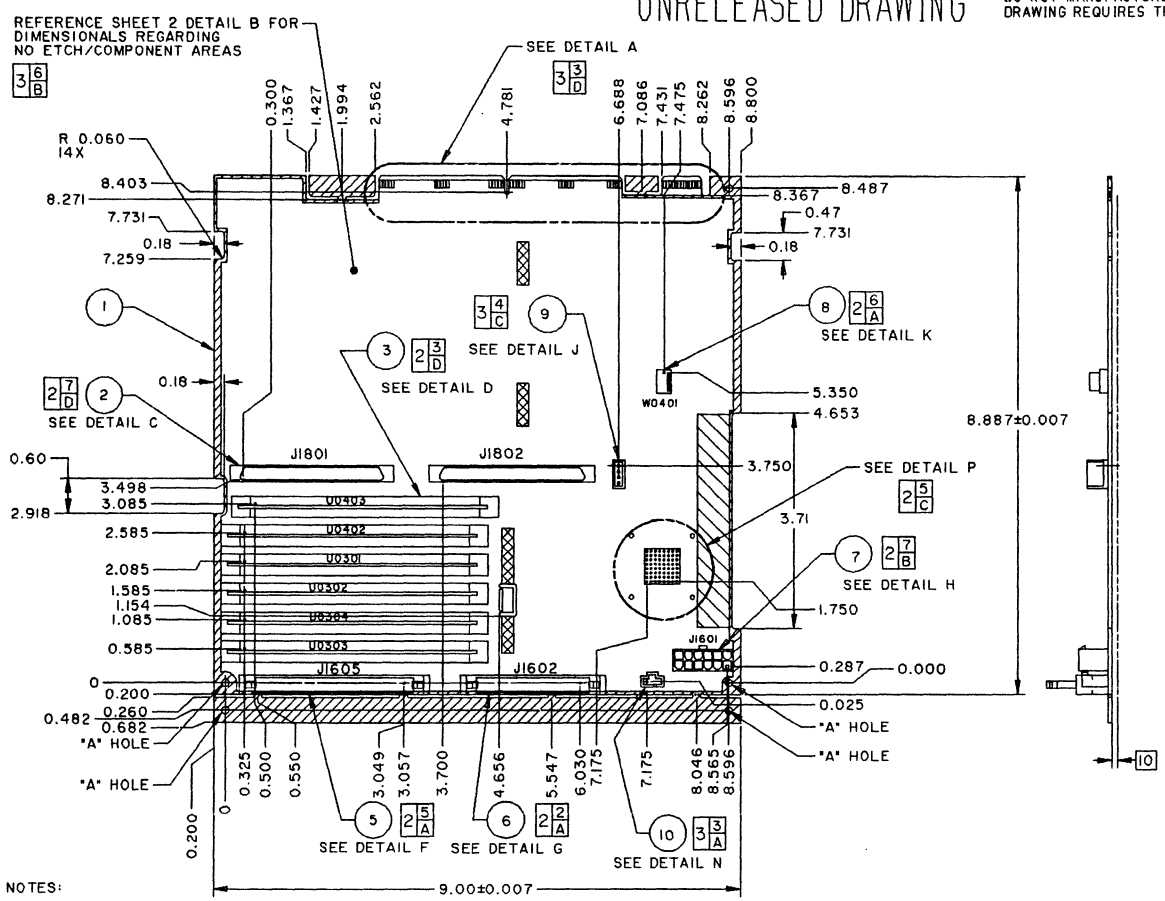
UNRELEASED DRAWING

DO NOT MANUFACTURE. ANY CHANGES TO THIS DRAWING REQUIRES THE APPROVAL OF _____

DWG NO.	SHT	REV

REVISIONS

BUFFA	REV.	DESCRIPTION	DATE	APPROVED
	01	INITIAL RELEASE	5-4-92	
	02	REVISE CONN LOC AUDIO, TSUNAMI, POWER	6-10-92	



HOLE LEGEND

SYM	DESCRIPTION	QTY
A	Ø0.125 ±0.003 NON-PTH	5
B	Ø0.035 ±0.003 PTH	84
C	Ø0.043 ±0.003 PTH	15
D	Ø0.076 ±0.002 NON-PTH	4
F	Ø0.040 ±0.002 PTH	432
G	Ø0.031 ±0.002 PTH	256
H	Ø0.062 +0.002/-0.000 NON-PTH	2
J	Ø0.096 +0.002/-0.000 NON-PTH	12
L	Ø0.116 ±0.002 NON-PTH	4
M	Ø0.055 ±0.002 PTH	12
N	Ø0.080 +0.002/-0.000 NON-PTH	6

NOTES:

1. ALL DIMENSIONS IN INCHES.
2. ALL DIMENSIONS LOCATING CONNECTORS TO PIN 1.
3. MATERIAL: EPOXY FIBERGLASS FR-4 UL FLAME RATING 94 VO.
4. TOLERANCES UNLESS OTHERWISE SPECIFIED:
   .XX = ±0.010
   .XXX = ±0.005
   ANGLES = ±0.5°
5. AREA TO BE FREE OF COMPONENTS, CHASSIS BAND ON TOP AND BOTTOM LAYERS.
6. AREA TO BE FREE OF COMPONENTS AND ETCH EXTERNAL LAYER ONLY. (FARSIDE)
7. MAXIMUM COMPONENT HEIGHT TO BE 0.250.
8. PCB SHALL BEAR UR APPROVAL MARKING, VENDOR DATE CODE AND COUNTRY OF ORIGIN.
9. EXTERNAL LAYERS TO HAVE GROUND ETCH ONLY (SOLDER MASK PERMISSABLE). INTERNAL LAYER SIGNAL RUNS TO BE 0.060 MINIMUM FROM EDGE.
10. MAXIMUM ALLOWABLE LEAD LENGTH TO BE 0.100.
11. BREAK AWAY TAB DIMENSIONS ARE FOR REF ONLY PCB VENDOR TO ENSURE FLUSH SURFACE FOLLOWING MATERIAL REMOVAL.

PART LIST

ITEM NO.	QTY REQD	PART OR IDENTIFYING NO.	APPROXIMATE DESCRIPTION	MATERIAL SPECIFIED
10	1	70543-0002	SINGLE ROW, 3 POS, .120 POCKET STR HDR	MOLEX
9	2	DFIB-4P-2.5DS	CONN, HDR, 4POS, 4 WALL, HIROSE	
8	1	130-1600-01	CONN, HDR, M, 4, VERT	
7	1	130-1427-01	CONN, HDR, M, 12, ENCLD, SN/SN	
6	1	499206-8	CONN, HDR, 34 POS, LATCHED, 4 WALL	AMP
5	1	499206-0	CONN, HDR.50 POS, LATCHED, 4 WALL	AMP
3	6	190-1144-01	SIMM SOCKET, MODULE	
2	2	130-1488-01	CONN, HDENS, F, 96, SPCL, EXT	
1	1	270-1851-01	BOARD, CPU, SUNERGY/C	

ENGLISH
THIRD ANGLE PROJECTION

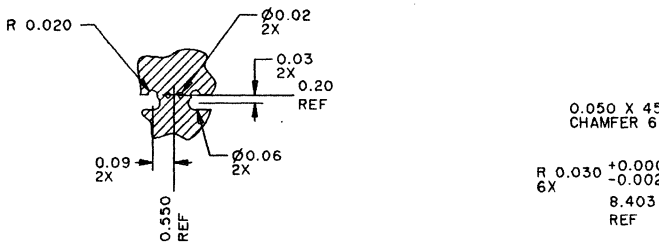
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS TOLERANCES ARE: DECIMALS .XX ±0.25 .XXX ±0.127 ANGLES ±1° — 4
MATERIAL — 3
FINISH N/A
DO NOT SCALE DRAWING

	APPROVALS	DATE
DRAWN	BOBA	02 MAY 92
CHECKED		
ENGR	BOBA	02 MAY 92
RELEASED		

sun microsystems

OUTLINE DRAWING, SUNERGY CLASSIC

SIZE D | DWG NO. 270-2077-50 | REV. 02
SCALE 1/1 | SHEET 1 OF 3



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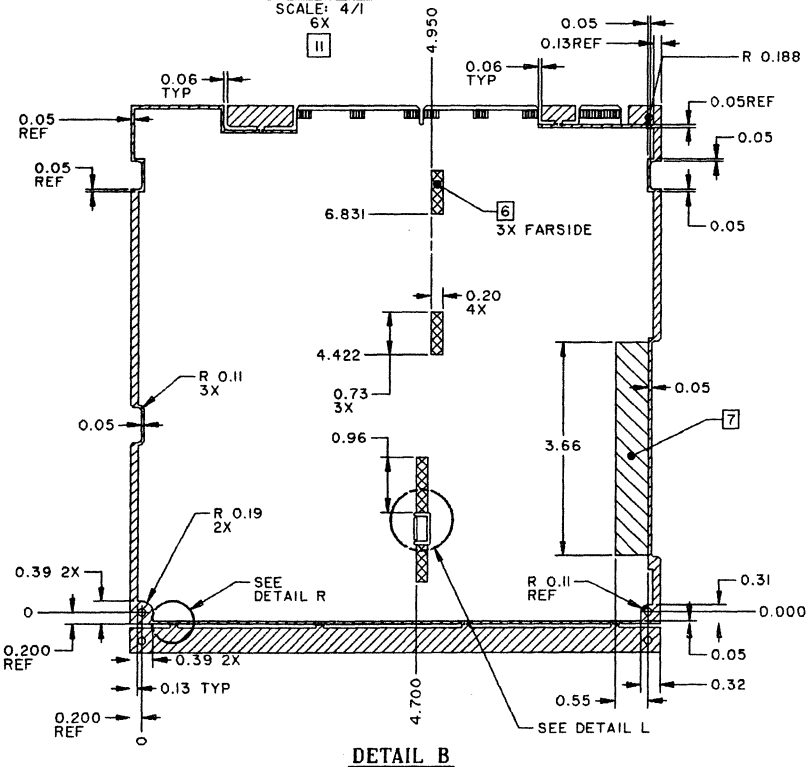

DETAIL B
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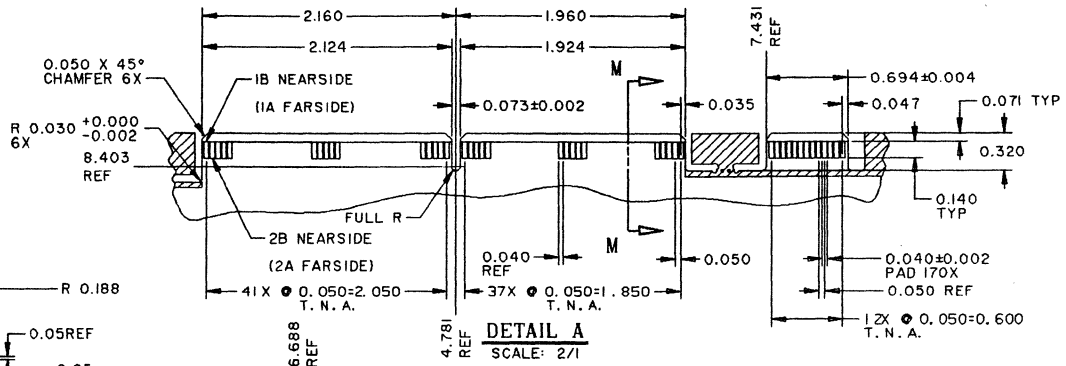
SOME DETAIL LEFT OUT
FOR CLARITY



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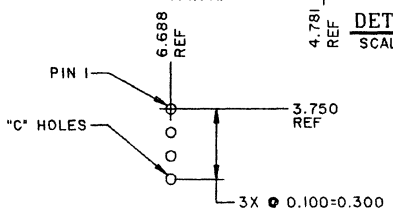

DETAIL J
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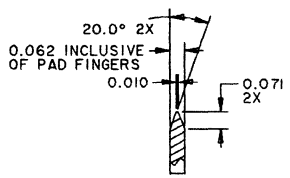

SECTION M-M
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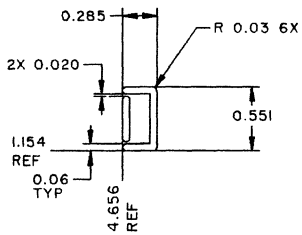

DETAIL L
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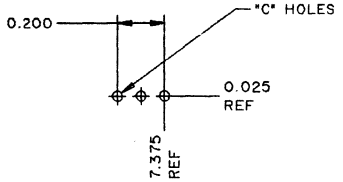
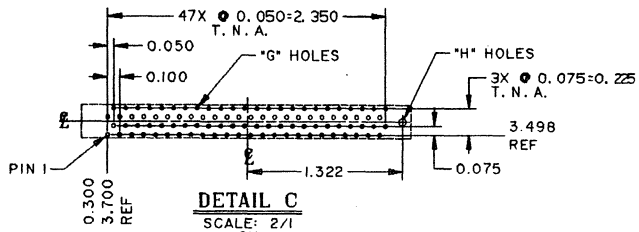


DETAIL N
SCALE: 4/1

sun	SIZE D	DWG NO. 270-2077-50	REV 02
	SCALE 1/1		SHEET 3 OF 3



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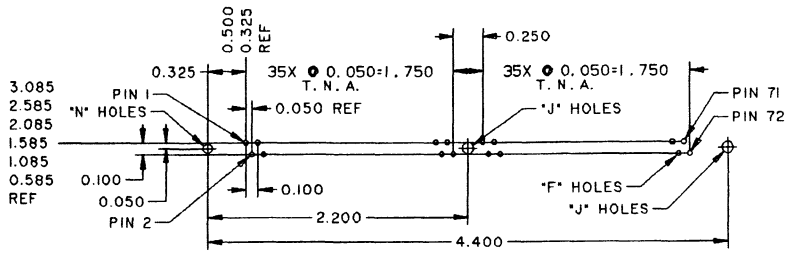

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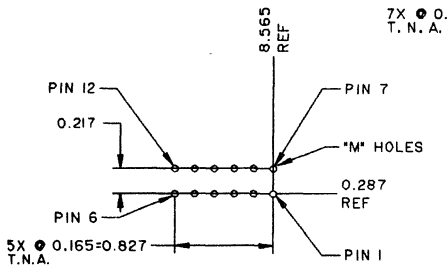

DETAIL H
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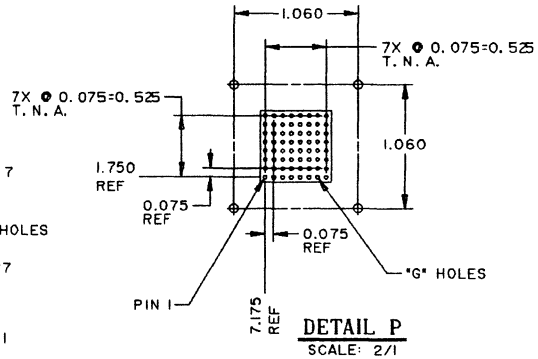

DETAIL P
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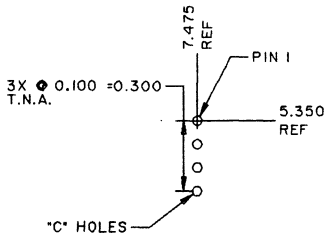

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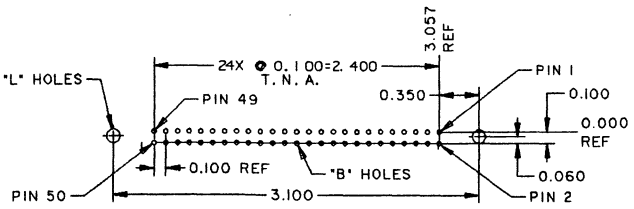

DETAIL F
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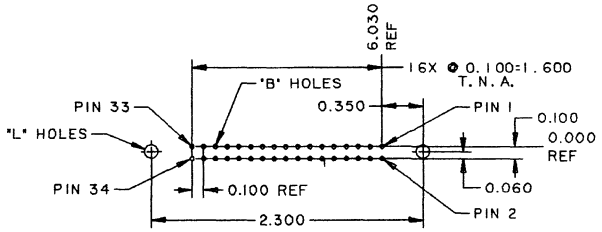


DETAIL G
SCALE: 2/1

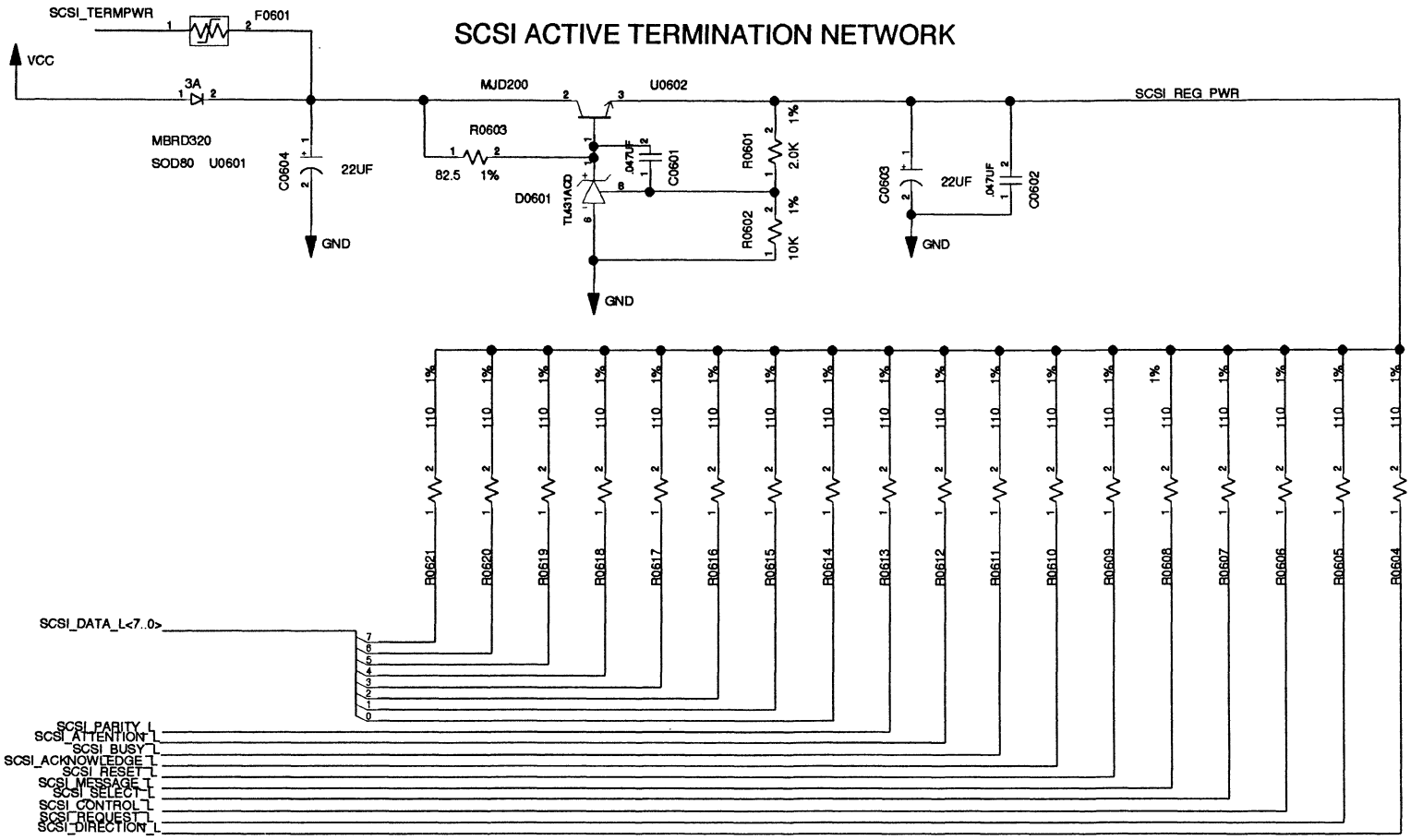
SPARCclassic Engine Schematics

B.1 SPARCclassic Engine Schematics

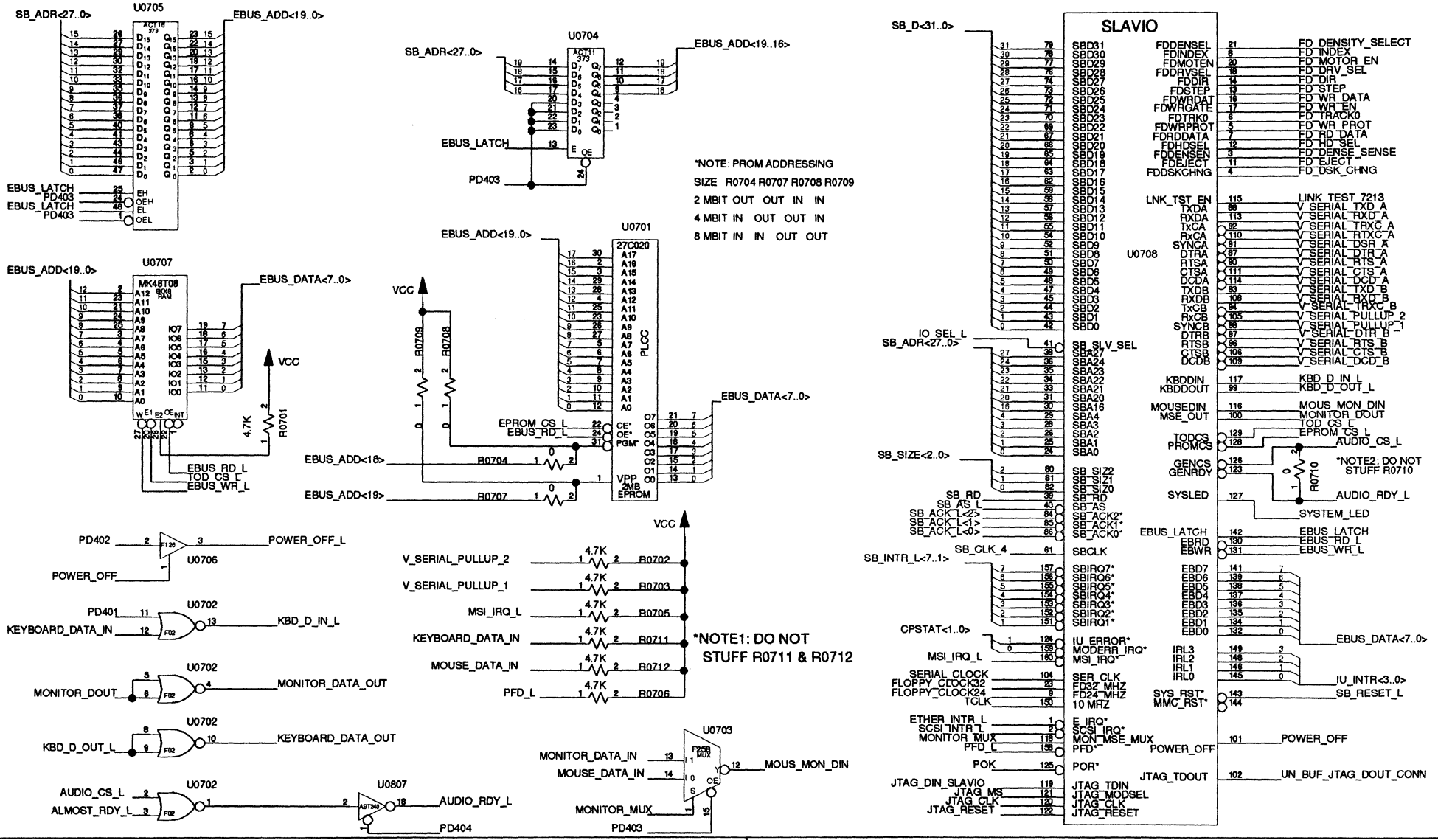
On the next few pages are selected pages from the SPARCclassic Engine board schematics. Included are pages 6, 7, 8, 12, 13, 14, 15, 16 and 17. Other pages of the schematics are not usually relevant to the development of SPARCclassic Engine-based products.

The complete set of schematics are available under non-disclosure. Please contact the Boards Marketing Group at Sun Microsystems to arrange for access to a complete set of schematics.

SCSI ACTIVE TERMINATION NETWORK

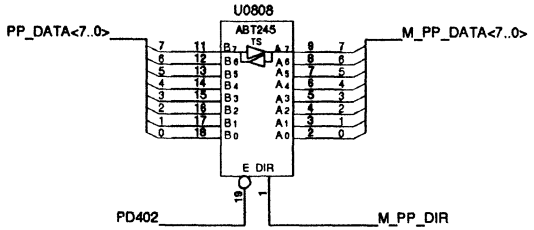


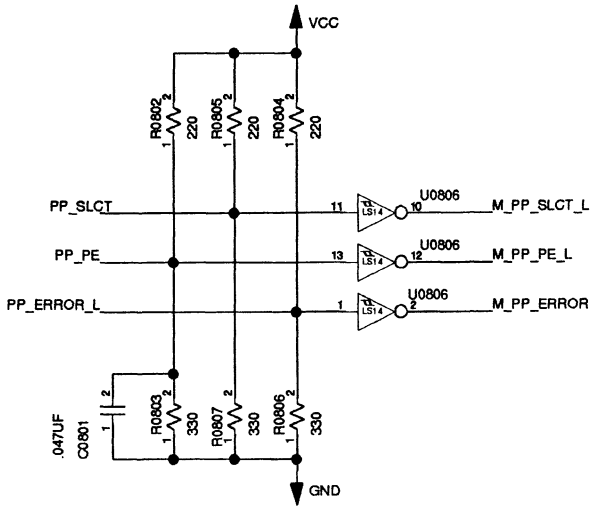
TITLE:	CLASSIC	SUNPARTNR:	502-2262-02	REV:	
SHEET:	6 OF 18		SCSI TERMINATION		P2.1
ENGINEER:	ANP	DATE:	AUGUST 29, 1992		

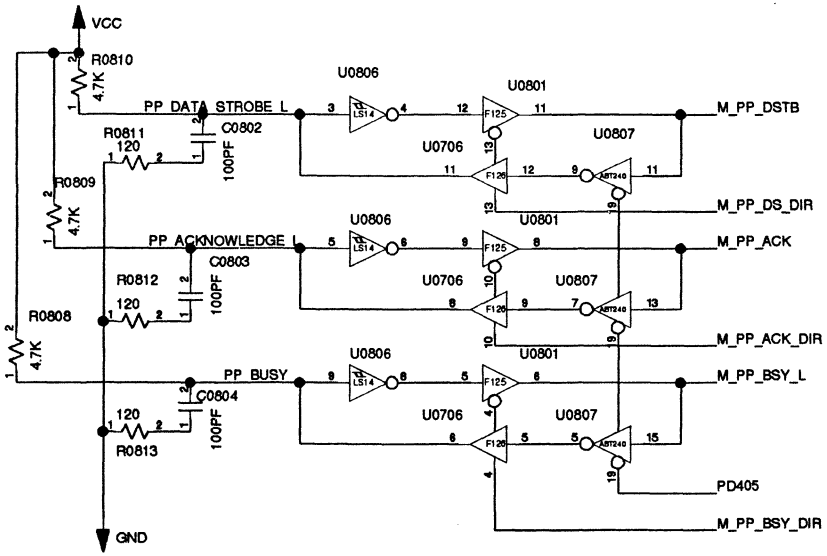


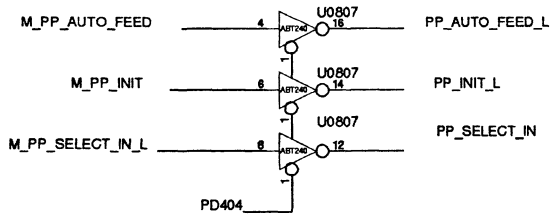
TITLE:	CLASSIC
SHEET:	7 OF 18
ENGINEER:	ANP
SUNPARTNR:	502-2262-02
	SLAVIO, PROM, NVRAM
DATE:	AUGUST 29, 1992
REV:	P2.1

PARALLEL PORT BUFFERS / TRANSCEIVERS

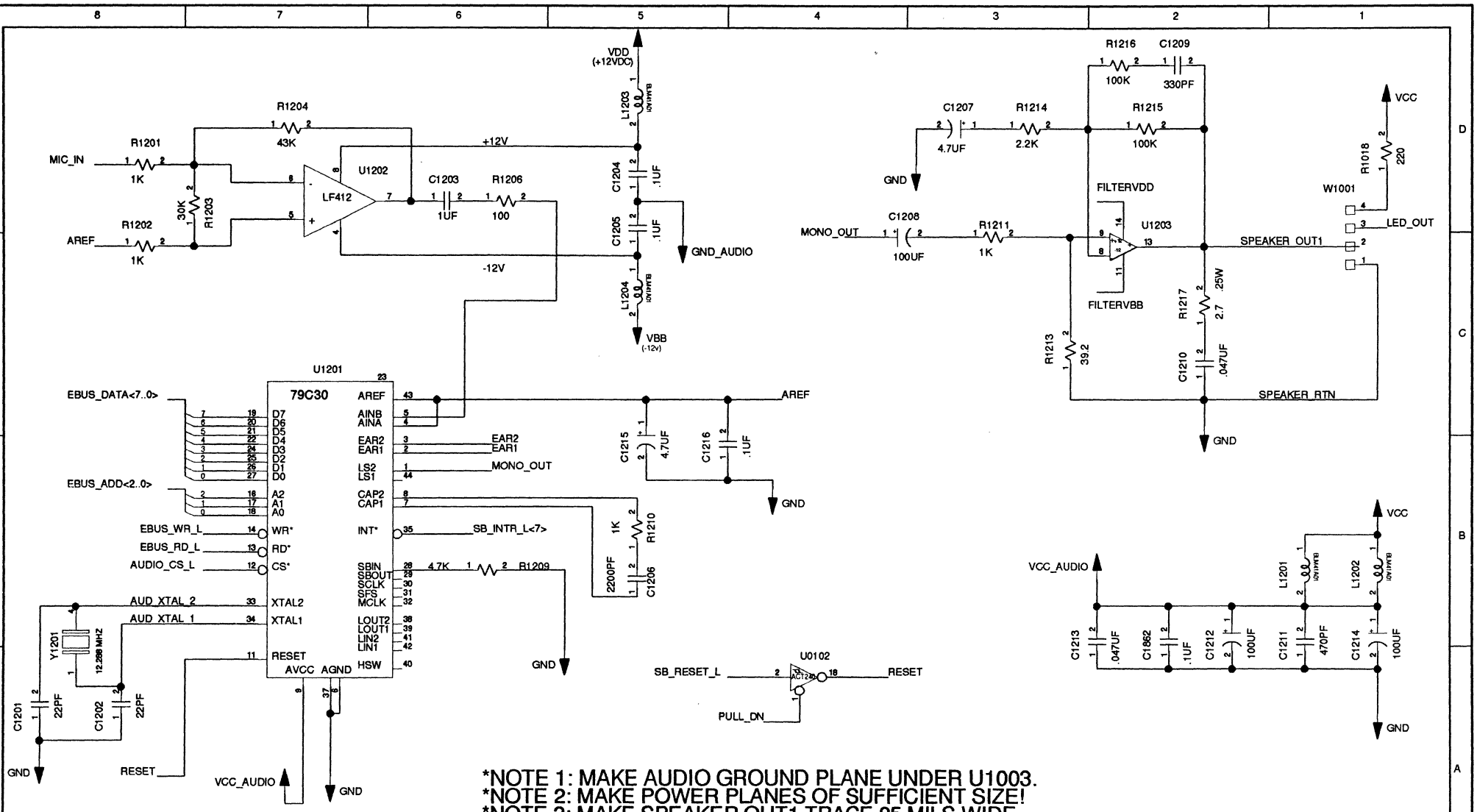








TITLE:	CLASSIC
SHEET:	8 OF 18
ENGINEER:	ANP
SUNPARTNR:	502-2077-02
	PARALLEL PORT
DATE:	AUGUST 29, 1992
REV:	P2.1



*NOTE 1: MAKE AUDIO GROUND PLANE UNDER U1003.
*NOTE 2: MAKE POWER PLANES OF SUFFICIENT SIZE!
*NOTE 3: MAKE SPEAKER OUT1 TRACE 25 MILS WIDE
*NOTE 4: MAKE SPEAKER_RTN TRACE 25 MILS WIDE

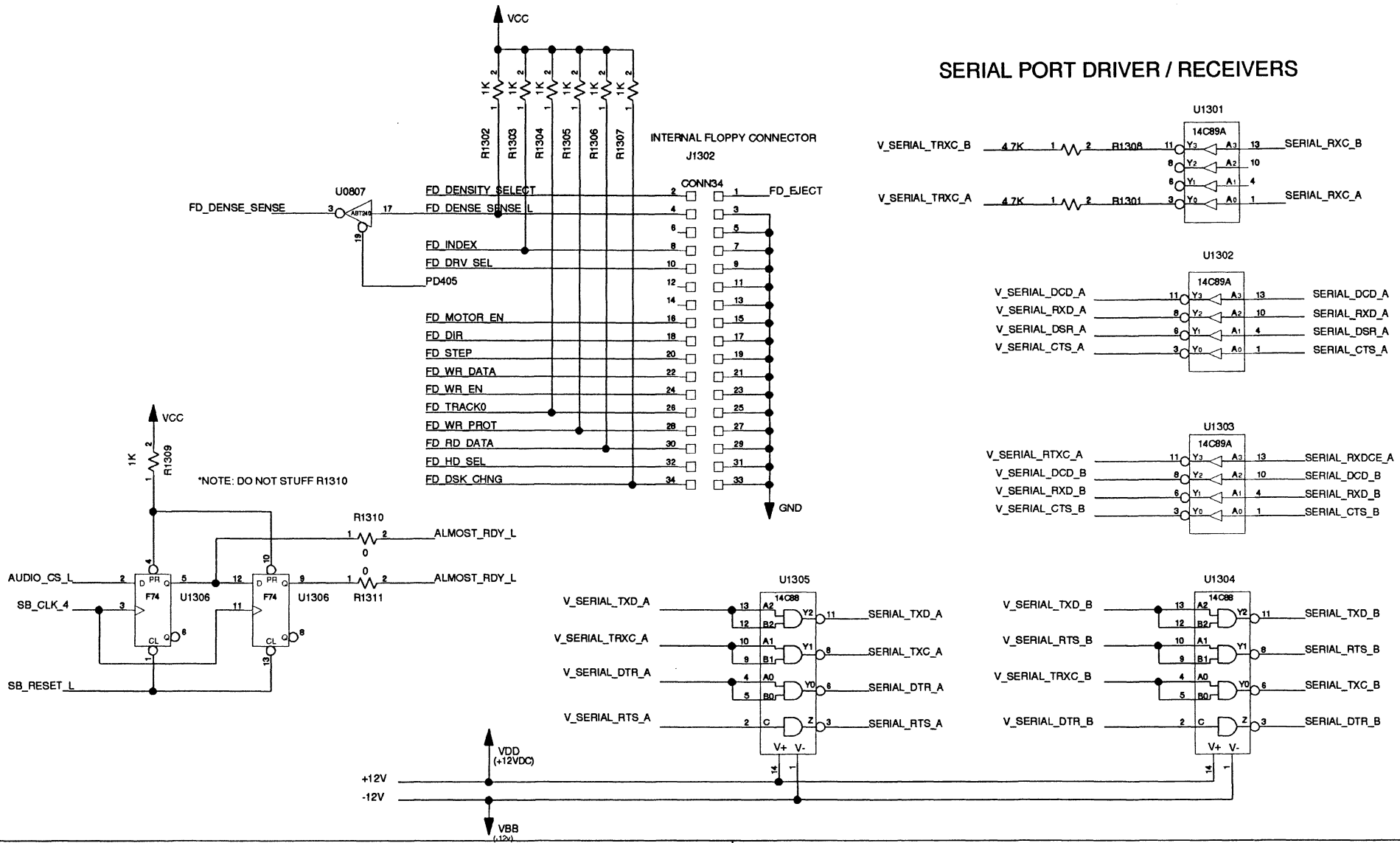
sun microsystems

TITLE: CLASSIC
SHEET: 12 OF 18
ENGINEER: ANP

SUNPARTNR: 502-2262-02
8-BIT AUDIO
DATE: AUGUST 29, 1992

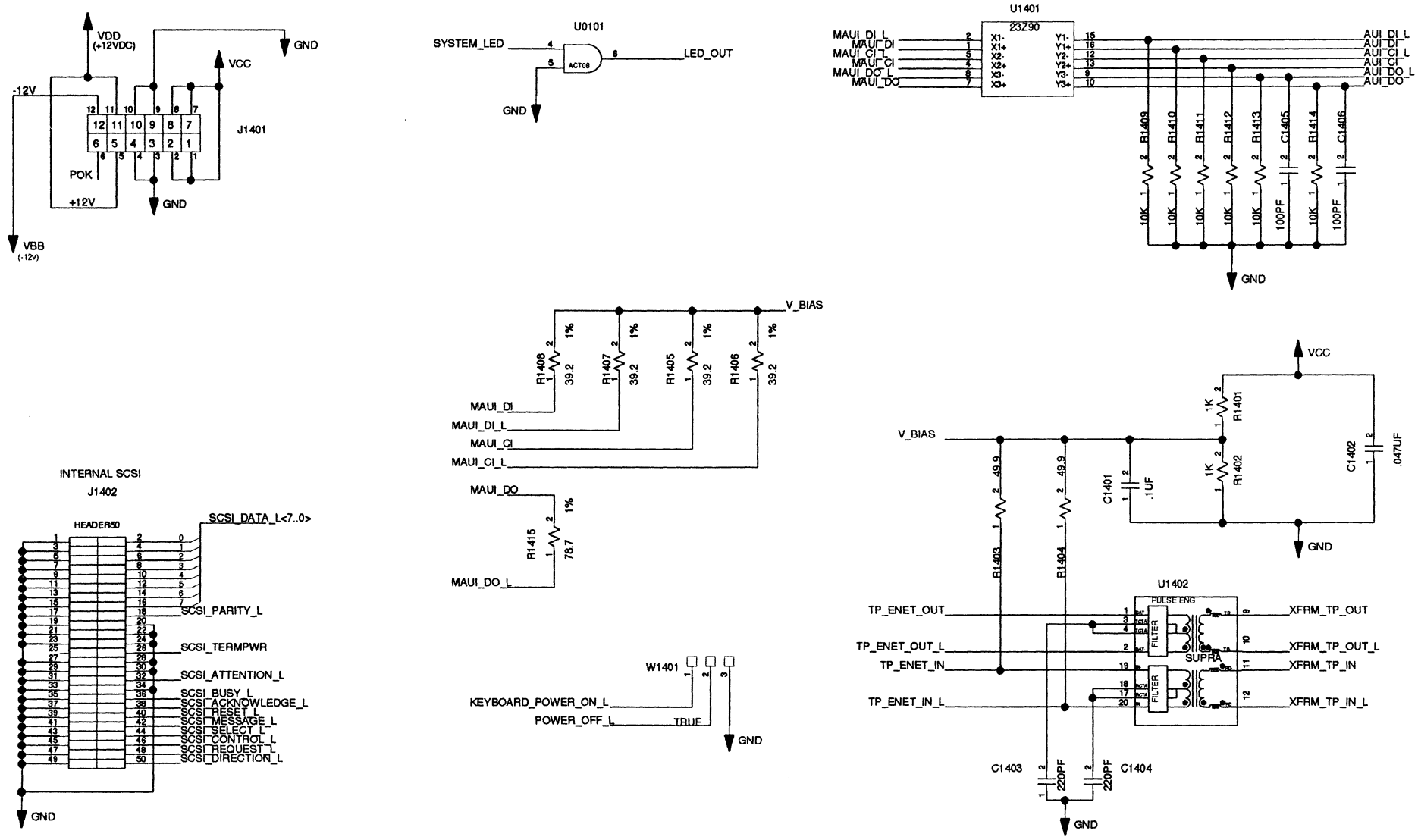
REV: P2.1

SERIAL PORT DRIVER / RECEIVERS



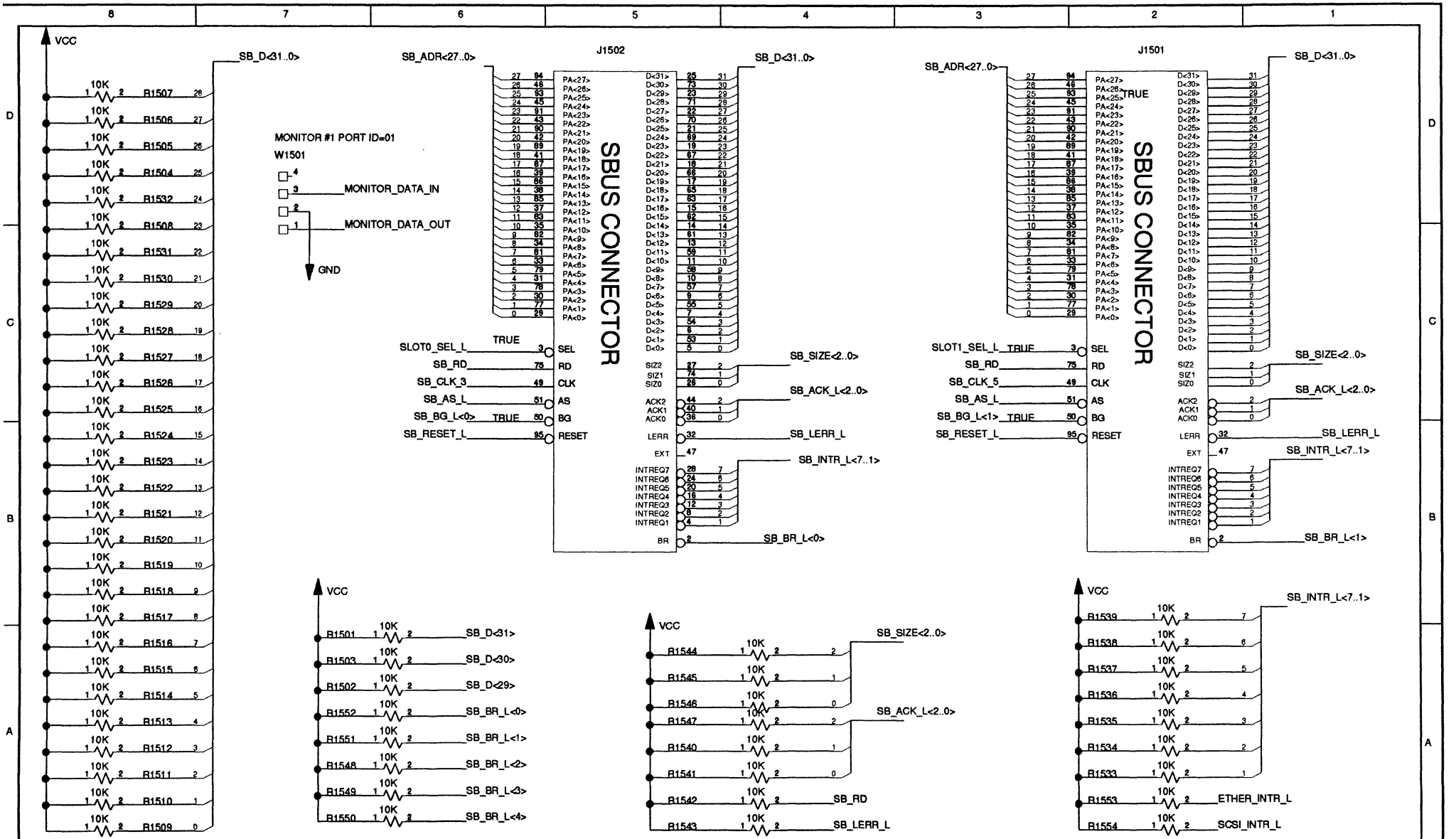
TITLE:	CLASSIC	SUNPARTNR:	502-2262-02
SHEET:	13 OF 18	REV:	P2.1
ENGINEER:	ANP	DATE:	AUGUST 29, 1992

SERIAL DRIVERS & RECEIVERS (RS232)

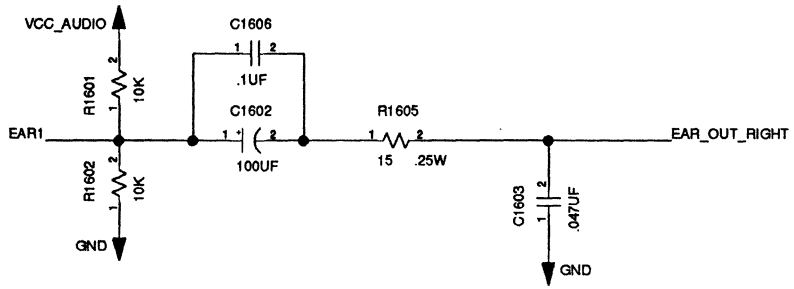


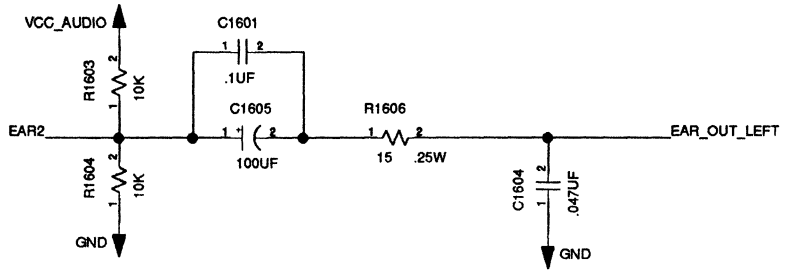
TITLE:	CLASSIC	SUNPARTNR:	502-2262-02
SHEET:	14 OF 18		ETHERNET,ETC
ENGINEER:	ANP	DATE:	AUGUST 29, 1992

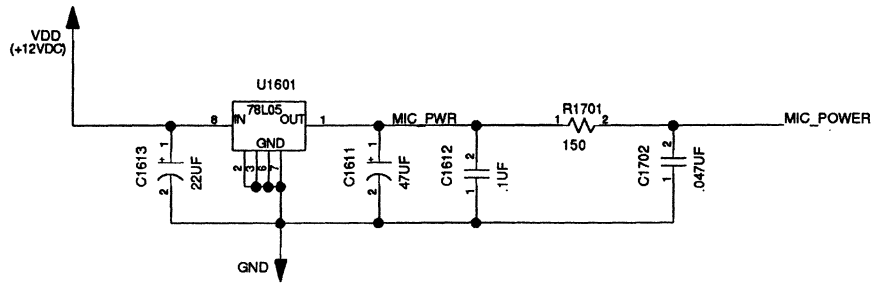
REV: P2.1



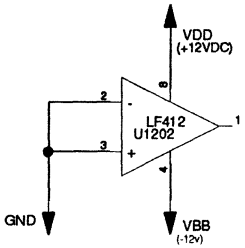
TITLE:	CLASSIC
SHEET:	15 OF 18
ENGINEER:	ANP
SUNPARTNR:	502-2262-02
	SBUS CONNECTORS
DATE:	AUGUST 29, 1992
REV:	P2.1

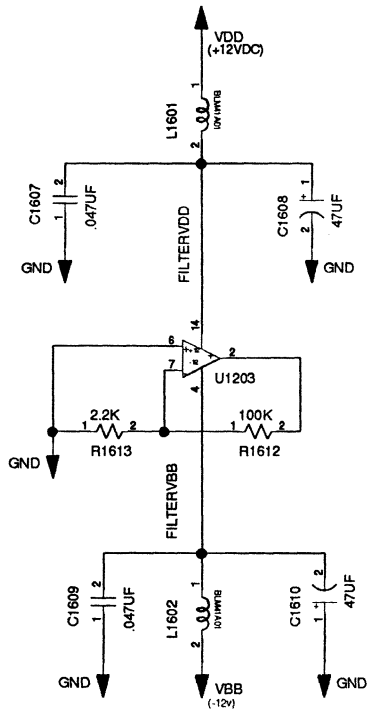






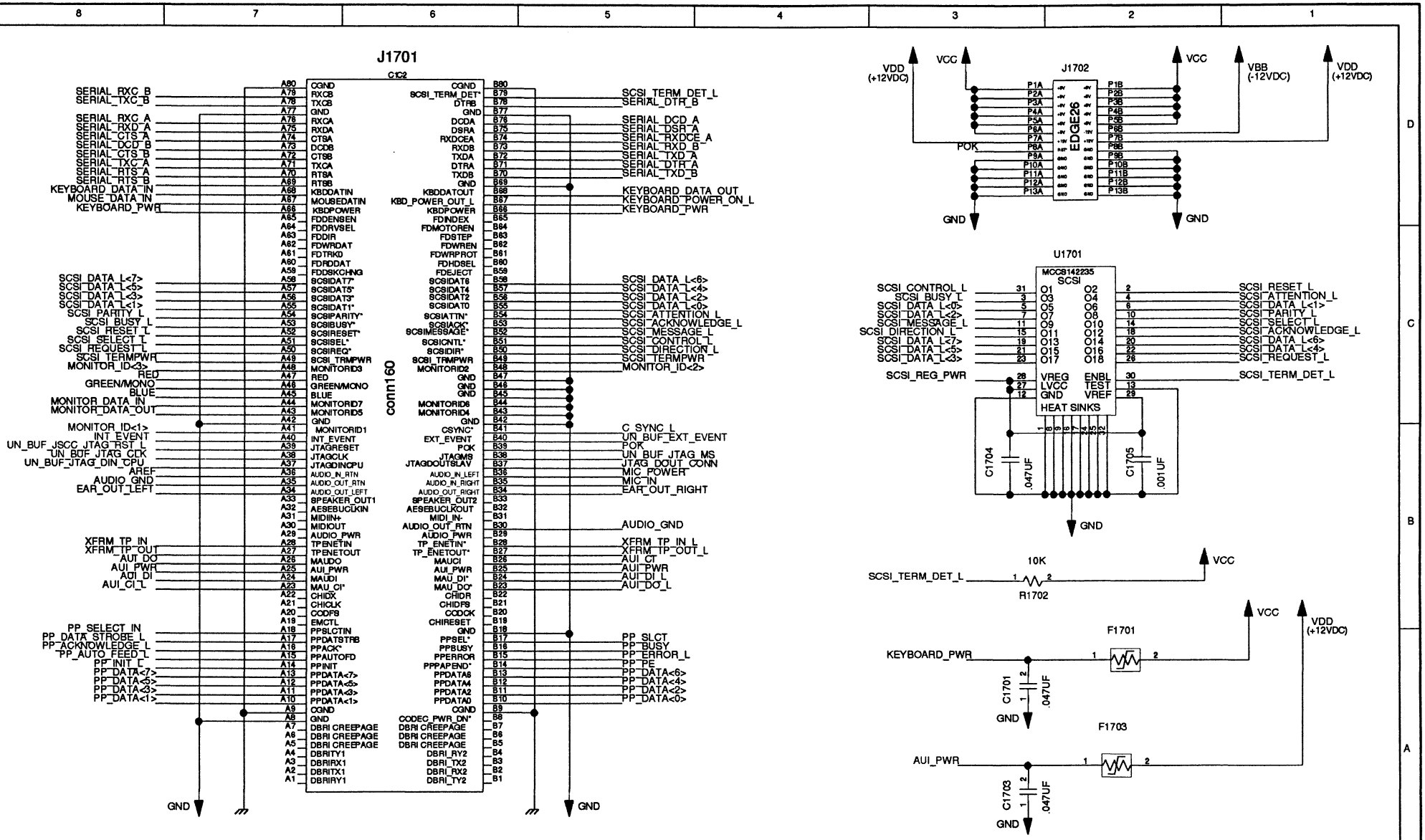
*NOTE: ALL AUDIO COMPONENTS ARE TO REMAIN IN CLOSE PROXIMITY TO POWER AMP AND AUDIO PLANES!





TITLE:	CLASSIC	SUNPARTNR:	502-2262-02
SHEET:	16 OF 18		HEADPHONE, MIC_PWR,SPARES
ENGINEER:	ANP	DATE:	AUGUST 29, 1992

REV: P2.1



TITLE:	CLASSIC	SUNPARTNR:	502-2262-02
SHEET:	17 OF 18		I/O CONNECTOR
ENGINEER:	ANP	DATE:	AUGUST 29, 1992

REV: P2.1

SPARCclassic Engine Pinouts

C.1 SBus Connectors Pinout List

Reference Identifiers: J1501/J1502

Connector Type: 96-pin female socket connector

Pin #	Signal	Pin #	Signal
1	gnd	49	clk
2	br*	50	bg*
3	sel*	51	as*
4	intreq1*	52	gnd
5	d0	53	d1
6	d2	54	d3
7	d4	55	d5
8	intreq2*	56	5V
9	d6	57	d7
10	d8	58	d9
11	d10	59	d11
12	intreq3*	60	gnd
13	d12	61	d13
14	d14	62	d15
15	d16	63	d17
16	intreq4*	64	5V
17	d19	65	d18
18	d21	66	d20
19	d23	67	d22
20	intreq5*	68	gnd

Pin #	Signal	Pin #	Signal
21	d25	69	d24
22	d27	70	d26
23	d29	71	d28
24	intreq6*	72	5V
25	d31	73	d30
26	siz0	74	siz1
27	siz2	75	rd
28	intreq7*	76	gnd
29	pa00	77	pa01
30	pa02	78	pa03
31	pa04	79	pa05
32	lerr*	80	select
33	pa06	81	pa07
34	pa08	82	pa09
35	pa10	83	pa11
36	ack0*	84	attention
37	pa12	85	pa13
38	pa14	86	pa15
39	pa16	87	pa17
40	ack1*	88	reset*
41	pa18	89	pa19
42	pa20	90	pa21
43	pa2	91	pa23
44	ack2*	92	request
45	pa24	93	pa25
46	pa26	94	pa27
47	n.c.	95	reset*
48	-12V	96	gnd

C.2 *SCSI Connector Pinout List*

Reference Identifier: J1402

Connector Type: 50-pin male socket transition connector

Signal	Pin #	Comments
GND	1	Ground
SD0	2	SCSI Data 0-
GND	3	Ground
SD1	4	SCSI Data 1-
GND	5	Ground
SD2	6	SCSI Data 2-
GND	7	Ground
SD3	8	SCSI Data 3-
GND	9	Ground
SD4	10	SCSI Data 4-
GND	11	Ground
SD5	12	SCSI Data 5-
GND	13	Ground
SD6	14	SCSI Data 6-
GND	15	Ground
SD7	16	SCSI Data 7-
GND	17	Ground
SDP	18	SCSI Parity-
GND	19	Ground
GND	20	Ground
GND	21	Ground
GND	22	Ground
GND	23	Ground
GND	24	Ground
NC	25	No Connect
TRMPWR	26	Terminator Power (~5 Volts DC, protected, 3 Amps)
GND	27	Ground
GND	28	Ground
GND	29	Ground
GND	30	Ground
GND	31	Ground

Signal	Pin #	Comments
ATN-	32	Attention-
GND	33	Ground
NC	34	No Connect
GND	35	Ground
BSY-	36	Busy-
GND	37	Ground
ACK-	38	Acknowledge-
GND	39	Ground
RST-	40	Reset-
GND	41	Ground
MSG-	42	Message-
GND	43	Ground
SEL-	44	Select-
GND	45	Ground
CD-	46	Command/Data-
GND	47	Ground
REQ-	48	Request-
GND	49	Ground
IO-	50	Input/Output-

Pin 38 is overcurrent-protected through a diode.

C.3 *Floppy Disk Drive Connector Pinout List*

Reference Identifier: J1302

Connector Type: 34-pin male dual-beam connector

Signal	Pin #	Description
FD_EJECT	1	Eject
FD_DENSITY_SELECT	2	density select
GND	3	Ground
FD_DENSE_SENSE_L	4	density sense l
GND	5	Ground
	6	index
GND	7	Ground
FD_INDEX	8	Index
GND	9	Ground
FD_DRV_SEL	10	drive select 0
GND	11	Ground
NC	12	No connect
GND	13	Ground
NC	14	No connect
GND	15	Ground
FD_MOTOR_EN	16	motor en
GND	17	Ground
FD_DIR	18	direction
GND	19	Ground
FD_STEP	20	step
GND	21	Ground
FD_WR_DATA	22	write data
GND	23	Ground
FD_WR_EN	24	write gate
GND	25	Ground
FD_TRACK0	26	track 0
GND	27	Ground
FD_WR_PROT	28	write protect
GND	29	Ground
FD_RD_DATA	30	read data
GND	31	Ground

Signal	Pin #	Description
FD_HD_SEL	32	hard disk select
GND	33	Ground
FD_DSK_CHNG	34	disk change

C.4 *160-Pin Male I/O Edge Connector Pinout List*

Reference Identifier: J1701

Connector Type: 160-pin male edge connector, two-row special

I/O Standard for SUNERGY	Pin #	SeSUNERGY Classic Board Signals
DBRIRY1	A1	DBRI_RY1
DBRITX1	A2	DBRI_TX1
DBRIRX1	A3	DBRI_RX1
DBRITY1	A4	DBRI_TY1
DBRI creepage	A5	
DBRI creepage	A6	
DBRI creepage	A7	
GND	A8	GND
CGND	A9	Chassis Ground
PPDATA<1>	A10	PP_DATA<1>
PPDATA<3>	A11	PP_DATA<3>
PPDATA<5>	A12	PP_DATA<5>
PPDATA<7>	A13	PP_DATA<7>
PPINIT	A14	PP_INIT_L
PPAUTOFD	A15	PP_AUTO_FEED_L
PPACK*	A16	PP_ACKNOWLEDGE_L
PPDATASTRB	A17	PP_DATA_STROBE_L
PPSLCTIN	A18	PP_SELECT_IN_L
EMCTL	A19	
CODFS	A20	
CHICLK	A21	
CHIDX	A22	
MAU_CI*	A23	AUI_CL_L
MAUDI	A24	AUI_DI
AUI_PWR	A25	AUI_PWR
MAUDO	A26	AUT_DO
TPENETOUT	A27	XFRM_TP_OUT
TPENETIN	A28	XFRM_TP_IN
AUDIO_PWR	A29	
MIDIOUT	A30	
MIDIIN+	A31	
AESEBUCLKIN	A32	

I/O Standard for SUNERGY	Pin #	SeSUNERGY Classic Board Signals
SPEAKER_OUT1	A33	
AUDIO_OUT_LEFT	A34	EAR_OUT_LEFT
AUDIO_OUT_RTN	A35	AUDIO_GND
AUDIO_IN_RTN	A36	AREF
JDTAGDINCPU	A37	UN_BUF_JTAG_DIN_CPU
JTAGCLK	A38	UN_BUF_JTAG_CLK
JTAGRESET	A39	UN_BUF_JSCC_JTAG_RESET
INT_EVENT	A40	INT_EVENT
MONITORID1	A41	MONITOR_ID<1>
GND	A42	GND
MONITORID5	A43	MONITOR_DATA_OUT
MONITORID7	A44	MONITOR_DATA_IN
BLUE	A45	BLUE
GREENMONO	A46	GREEN/MONO
RED	A47	RED
MONITORID3	A48	MONTITOR_ID<3>
SCSI_TRMPWR	A49	SCSI_TRMPWR
SCSIREQ*	A50	SCSI_REQUEST_L
SCSISEL*	A51	SCSI_SELECT_L
SCSIRESET*	A52	SCSI_RESET_L
SCSIBUSY*	A53	SCSI_BUSY_L
SCSIPARITY*	A54	SCSI_PARITY_L
SCSIDAT1*	A55	SCSI_DATA_L<1>
SCSIDAT3*	A56	SCSI_DATA_L<3>
SCSIDAT5*	A57	SCSI_DATA_L<5>
SCSIDAT7*	A58	SCSI_DATA_L<7>
FFDSKCHNG	A59	
FDRDDAT	A60	
FDTRK0	A61	
FDWRDAT	A62	
FDDIR	A63	
FDDRVSEL	A64	
FDDENSEN	A65	
KBDPOWER	A66	KEYBOARD_PWR
MOUSEDATIN	A67	MOUSE_DATA_IN
KBDATIN	A68	KEYBOARD_DATA_IN
RTSB	A69	SERIAL_RTS_B
RTSA	A70	SERIAL_RTS_A

I/O Standard for SUNERGY	Pin #	SeSUNERGY Classic Board Signals
TXCA	A71	SERIAL_TXC_A
CTSB	A72	SERIAL_CTS_B
DCDB	A73	SERIAL_DCD_B
CTSA	A74	SERIAL_CTS_A
RXDA	A75	SERIAL_RXD_A
RXCA	A76	SERIAL_RXC_A
GND	A77	GND
TXCB	A78	SERIAL_TXC_B
RXCB	A79	SERIAL_RXC_B
CGND	A80	
DBRITY2	B1	
DBRIRX2	B2	
DBRITX2	B3	
DBRIRY2	B4	
DBRI creepage	B5	
DBRI creepage	B6	
DBRI creepage	B7	
FCODEC_PWR_DN*	B8	
CGND	B9	Chassis Ground
PPDaTA<0>	B10	PP_DATA<0>
PPDATA<2>	B11	PP_DATA<2>
PPDATA<4>	B12	PP_DATA<4>
PPDATA<6>	B13	PP_DATA<6>
PPPAPEND*	B14	PP_PE
PPERROR	B15	PP_ERROR_L
PPBUSY	B16	PP_BUSY
PPSEL*	B17	PP_SLCT
GND	B18	GND
CHIRESET	B19	
CODCK	B20	
CHIDFS	B21	
CHIDR	B22	
MAU_DO*	B23	AUI_DO_L
MAU_DI*	B24	AUI_DI_L
AUI_PWR	B25	AUI_PWR
MAUCI	B26	AUI_CI
TP_ENETOUT*	B27	XFRM_TP_OUT_1
TP_ENETIN*	B28	XFRM_TP_IN_L

I/O Standard for SUNERGY	Pin #	SeSUNERGY Classic Board Signals
AUDIO_PWR	B29	
AUDIO_OUT_RTN	B30	AUDIO_GND
MIDI_IN-	B31	
AESEBUCLKOUT	B32	
SPEAKER_OUT2	B33	
AUDIO_OUT_RIGHT	B34	EAR_OUT_RIGHT
AUDIO_IN_RIGHT	B35	MIC_IN
AUDIO_IN_LEFT	B36	MIC_PWR
JDTAGDOUTSLAV	B37	JTAG_DOUT_CONN
JTAGMS	B38	UN_BUF_JTAG_MS
POK	B39	POK
EXT_EVENT	B40	UN_BUF_EXT_EVENT
CSYNC*	B41	CSYNC_L
GND	B42	GND
MONITORID4	B43	GND
MONITORID6	B44	GND
GND	B45	GND
GND	B46	GND
GND	B47	GND
MONITORID2	B48	MONTITOR_ID<2>
SCSI_TRMPWR	B49	SCSI_TRMPWR
SCSIDIR*	B50	SCSI_DIRECTION_L
SCSICNTL*	B51	SCSI_CONTROL_L
SCSIMESSAGE*	B52	SCSI_MESSAGE_L
SCSIIACK*	B53	SCSI_ACKNOWLEDGE_L
SCSIATTN*	B54	SCSI_ATTENTION_L
SCSIDAT0*	B55	SCSI_DATA_L<0>
SCSIDAT2*	B56	SCSI_DATA_L<2>
SCSIDAT4*	B57	SCSI_DATA_L<4>
SCSIDAT6*	B58	SCSI_DATA_L<6>
FDEJECT	B59	
FDHDSEL	B60	
FDWRPROT	B61	
FDWWRENT	B62	
FDSTEP	B63	
FDMOTOREN	B64	
FDINDEX	B65	
KBDPOWER	B66	KEYBOARD_PWR

I/O Standard for SUNERGY	Pin #	SeSUNERGY Classic Board Signals
KBD_POWER_OUT_L	B67	KBD_POWER_ON_L
KBDDATOUT	B68	KEYBOARD_DATA_OUT
GND	B69	GND
TXDB	B70	SERIAL_TXD_B
DTRA	B71	SERIAL_DTR_A
TXDA	B72	SERIAL_TXD_A
RXDB	B73	SERIAL_RDX_B
RXDCEA	B74	SERIAL_RDDCE_A
DSRA	B75	SERIAL_DSR_A
DCDA	B76	SERIAL_DCD_A
GND	B77	GND
DTRB	B78	SERIAL_DTR_B
NC	B79	Not Connected
CGND	B80	Chassis Ground

C.5 LED & Speaker Out Connector Pinout List

Reference Identifier: W1001

Connector Type: 4-pin male connector, no housing

Signal	Pin #	Comments
GND	1	Ground
SPEAKER_OUT1	2	
LED_OUT	3	
VCC	4	

C.6 Power Connector Pinout List

Reference Identifier: J1401

Connector Type: 12-pin male mini-fit connector

Signal	Pin #	Comments
VCC	1	+5VDC
VCC	2	+5VDC
Ground	3	
Ground	4	
VDD	5	+12VDC
POK	6	
VCC	7	+5VDC
VCC	8	+5VDC
Ground	9	
Ground	10	
VDD	11	+12VDC
VBB	12	-12VDC

C.7 *Power Edge Connector Pinout List*

Reference Identifier: J1702

Connector Type: 26-pin male edge connector

Signal	Pin #	Comments
VCC	P1A	
VCC	P2A	
VCC	P3A	
VCC	P4A	
VCC	P5A	
VCC	P6A	
VDD	P7A	+12VDC
POR	P8A	Power-on Reset
GND	P9A	Ground
GND	P10A	Ground
GND	P11A	Ground
GND	P12A	Ground
GND	P13A	Ground
VCC	P1B	
VCC	P2B	
VCC	P3B	
VCC	P4B	
VCC	P5B	
VBB	P6B	-12VDC
VDD	P7B	+12VDC
GND	P8B	Ground
GND	P9B	Ground
GND	P10B	Ground
GND	P11B	Ground
GND	P12B	Ground
GND	P13B	Ground

C.8 *Monitor Connector Pinout List*

Reference Identifier: W1501

Connector Type: 4-pin male connector, no housing

Signal	Pin #	Comments
MONITOR_DATA_OUT	1	
MONITOR_DATA_IN	2	
GND	3	Ground
NC	4	Not Connected

C.9 *Power On/Off Connector Pinout List*

Reference Identifier: W1401

Connector Type: 3-pins, no housing

Signals	Pin #	Comments
KEYBOARD_POWER_ON_L	1	
POWER_OFF_L	2	
GND	3	Ground

C.10 *DRAM Connectors Pinout List*

Reference Identifiers: U0301/U0302/U0303/U0304/U0401/U0402

Connector Type: 72-pin female vertical micro-edge connector

See the DRAM specifications in **Appendices D and E.**

DRAM Specifications (4 MB)

On the next few pages are the SPARCclassic Engine 4 MB DRAM mechanical drawings and specification. Use the drawings to determine the product size and shape.

DISCLAIMER: Sun Microsystems does not endorse the product as defined in the following specification. The specification is provided for information purposes only.

DISCLAIMER: The manufacturer of the product specified in the next few pages does not accept any implied warranty other than is provide with the product itself under their own purchasing agreements.

NEW PRODUCT

SUN MICRO

HB56A133SU-6A

1,048,576-Word×33-Bit High Density Dynamic RAM Module

Rev.3
Mar,03,1992

HITACHI

Description

HB56A133SU6A is a 1M×33 dynamic RAM module, mounted 9 pieces of 4Mbit DRAM (HM514400AS) sealed in SOJ package.

An outline of this module is 72-pin single in-line package.

Therefore, HB56A133SU6A makes high density mounting possible without surface mount technology. HB56A133SU provides common data inputs and outputs.

Decoupling capacitors are mounted beneath each SOJ.

■ Feature

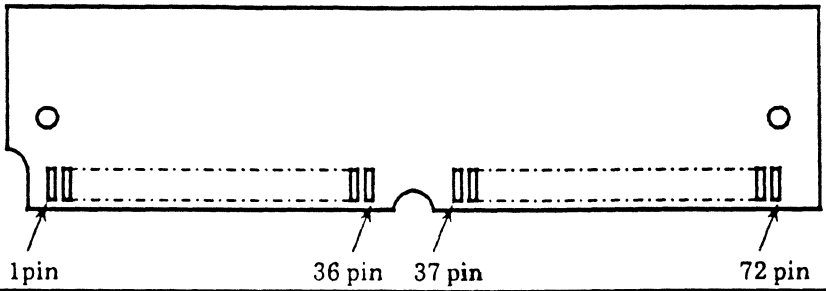
- 72-pin single in-line package
  - Lead pitch 1.27mm
- Single 5V (± 5%) supply
- High speed
  - Access time ..... 60ns (max)
- Low power dissipation
  - Active mode ..... 5.20W (max)
  - Standby mode ..... 94.5mW(max)
- Fast page mode capability
- 1,024refresh cycle / 8ms
- 2 variations of refresh
  - $\overline{RAS}$ only refresh
  - $\overline{CAS}$ before $\overline{RAS}$ refresh
- TTL compatible

■ Ordering information

Access time	Package
60ns	72-pin SIP Socket type

Preliminary : This document contains information on a new product. Specifications and information contained herein are subject to change without notice.
新製品のデータシートです。掲載内容は,予告なく変更,廃止されることがあります。

■ Pin Out



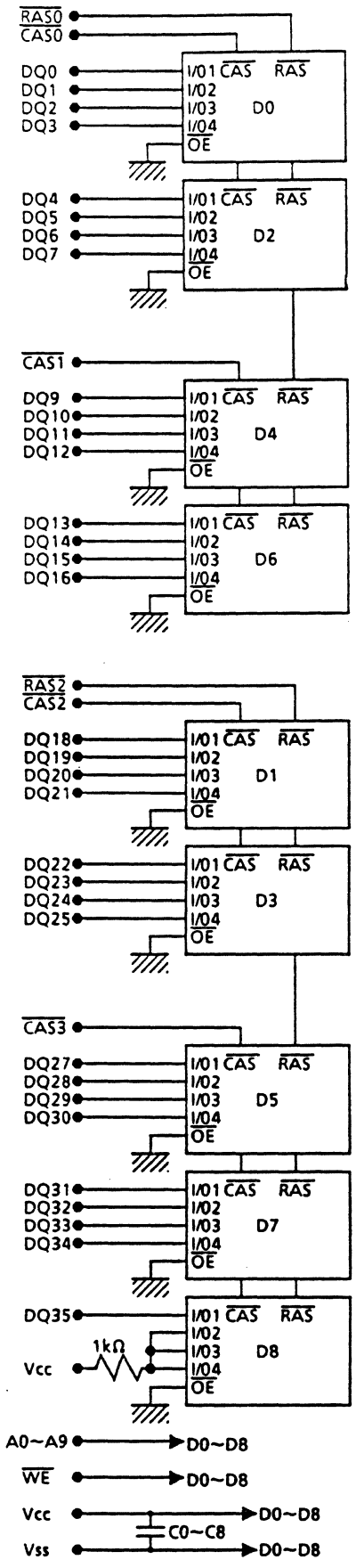
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	19	NC	37	NC	55	DQ12
2	DQ0	20	DQ4	38	DQ35	56	DQ30
3	DQ18	21	DQ22	39	V_{SS}	57	DQ13
4	DQ1	22	DQ5	40	$\overline{CAS0}$	58	DQ31
5	DQ19	23	DQ23	41	$\overline{CAS2}$	59	V_{CC}
6	DQ2	24	DQ6	42	$\overline{CAS3}$	60	DQ32
7	DQ20	25	DQ24	43	$\overline{CAS1}$	61	DQ14
8	DQ3	26	DQ7	44	$\overline{RAS0}$	62	DQ33
9	DQ21	27	DQ25	45	NC	63	DQ15
10	V_{CC}	28	A7	46	NC	64	DQ34
11	NC	29	NC	47	$\overline{WE}$	65	DQ16
12	A0	30	V_{CC}	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	V_{SS}*
14	A2	32	A9	50	DQ27	68	V_{SS}*
15	A3	33	NC	51	DQ10	69	NC*
16	A4	34	$\overline{RAS2}$	52	DQ28	70	NC*
17	A5	35	NC	53	DQ11	71	NC
18	A6	36	NC	54	DQ29	72	V_{SS}

* Presense detect pin using jumper-chip.

■ Pin Description

Pin Name	Function
A0 to A9	Address Input
A0 to A9	Refresh Address Input
DQ0 to DQ35	Data-in / Data-out
$\overline{CAS0}$ to $\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$,$\overline{RAS2}$	Row Address Strobe
$\overline{WE}$	Read / Write Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
NC	Non-connection

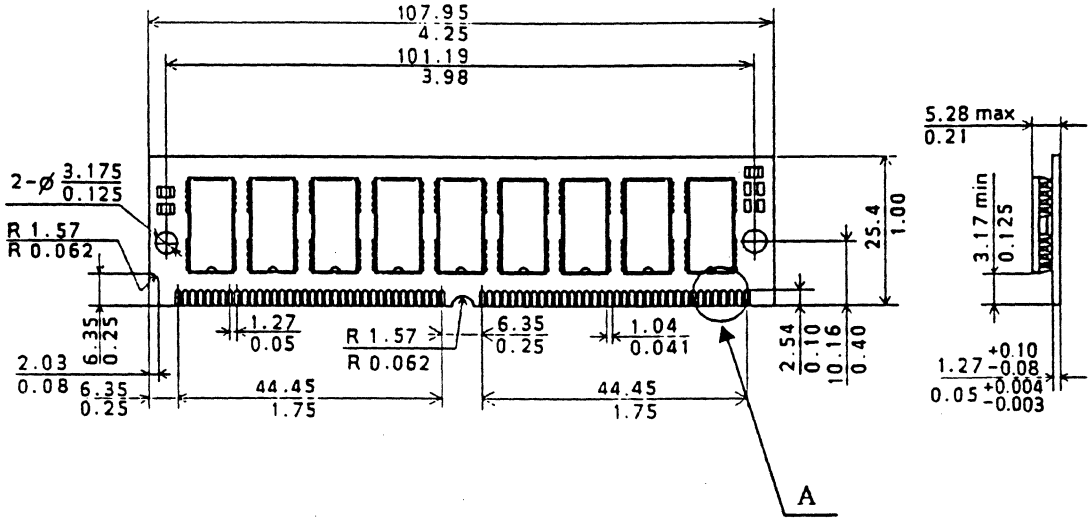
■ Block Diagram



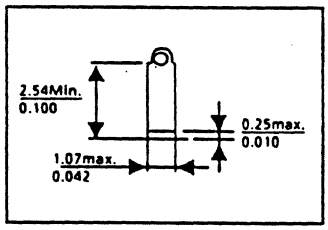
D0~D8 : HM514400AS

■ Physical Outline

Unit : mm / inch



Detail A



■ Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	(Input)	V_{IN}	−1.0 to +7.0	V
	(Output)	V_{OUT}	−1.0 to +7.0	V
Supply voltage relative to V_{SS}		V_{CC}	−1.0 to +7.0	V
Short circuit output current		I_{out}	50	mA
Power dissipation		P_T	9	W
Operating temperature		T_{opr}	0 to +70	°C
Storage temperature		T_{stg}	−55 to +125	°C

■ Electrical Characteristics

☆ Recommended DC Operating Conditions (T_a=0 to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	V_{IH}	2.4	−	5.5	V	1
Input low voltage	V_{IL}	−1.0	−	0.8	V	1

Note : 1. All voltage referenced to V_{SS}

☆ DC Electrical Characteristics ($Ta = 0$ to $+70°C$, $V_{CC} = 5V \pm 5\%$, $V_{SS} = 0V$)

Parameter	Symbol	60ns		Unit	Test Condition	Note
		Min.	Max.			
Operating current	I_{CC1}	–	990	mA	t_{RC} = min	1,2
Standby current	I_{CC2}	–	18	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{OUT} = High-Z	
		–	9	mA	CMOS interface $\overline{RAS}$, $\overline{CAS} \geqq V_{CC} - 0.2V$ D_{OUT} = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	–	990	mA	t_{RC} = min	2
Standby current	I_{CC5}	–	45	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{OUT} = enable	1
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC6}	–	990	mA	t_{RC} = min	
Page mode current	I_{CC7}	–	990	mA	t_{PC} = min	1,3
Input leakage current	I_{LI}	−10	10	μA	$0V \leqq V_{IN} \leqq 7V$	
Output leakage current	I_{LO}	−10	10	μA	$0V \leqq V_{OUT} \leqq 7V$ D_{OUT} = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	V	High $I_{OUT} = -5mA$	
Output low voltage	V_{OL}	0	0.4	V	Low $I_{OUT} = 4.2mA$	

Note : 1 . I_{CC} depends on output load condition when the device is selected , I_{CC} max is specified at the output open condition.

2 . Address can be changed less than three times while $\overline{RAS} = V_{IL}$.

3 . Address can be changed once or less while $\overline{CAS} = V_{IH}$.

☆ Capacitance ($Ta = 25°C$, $V_{CC} = 5V \pm 5\%$)

Parameter	Symbol	60ns		Unit	Note
		Typ.	Max.		
Input capacitance (Address)	C_{I1}	–	73	pF	1
Input capacitance ($\overline{WE}$)	C_{I2}	–	83	pF	1
Input capacitance ($\overline{RAS}$)	C_{I3}	–	50	pF	1
Input capacitance ($\overline{CAS}$)	C_{I4}	–	36	pF	1
Output capacitance (DQ0 – 7, 9 – 16, 18 – 25, 27 – 35)	$C_{I/O}$	–	17	pF	1, 2

Note : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS} = V_{IH}$ to disable D_{OUT}.

☆ AC Characteristics ($Ta = 0$ to $70°C$, $V_{CC} = 5V \pm 5\%$, $V_{SS} = 0V$) 1), 12)

- Read, write and refresh cycle (Common parameters)

Parameter	Symbol	60ns		Unit	Note
		Min.	Max.		
Ramdom read or write cycle time	t_{RC}	110	–	ns	
$\overline{RAS}$ precharge time	t_{RP}	40	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10000	ns	
Row address set-up time	t_{ASR}	0	–	ns	
Row address hold time	t_{RAH}	10	–	ns	
Column address set-up time	t_{ASC}	0	–	ns	
Column address hold time	t_{CAH}	15	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	ns	8
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	ns	9
$\overline{RAS}$ hold time	t_{RSH}	15	–	ns	
$\overline{CAS}$ hold time	t_{CSH}	60	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	ns	
Transition time (rise and fall)	t_T	3	50	ns	7
Refresh period	t_{REF}	–	8	ms	15

- Read cycle

Parameter	Symbol	60ns		Unit	Note
		Min.	Max.		
Access time from $\overline{RAS}$	t_{RAC}	–	60	ns	2,3
Access time from $\overline{CAS}$	t_{CAC}	–	15	ns	3,4
Access time from address	t_{AA}	–	30	ns	3,5
Read command set-up time	t_{RCS}	0	–	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	–	ns	
Read command hold time to $\overline{RAS}$	t_{RRH}	0	–	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	–	ns	
Output buffer turn-off time	t_{OFF}	–	15	ns	6

- Write cycle

Parameter	Symbol	60ns		Unit	Note
		Min.	Max.		
Write command set-up time	t_{WCS}	0	–	ns	10
Write command hold time	t_{WCH}	15	–	ns	
Write command pulse width	t_{WP}	10	–	ns	
Data-in set-up time	t_{DS}	0	–	ns	11
Data-in hold time	t_{DH}	15	–	ns	11

- Refresh cycle

Parameter	Symbol	60ns		Unit	Note
		Min.	Max.		
$\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$ refresh cycle)	t_{CSR}	10	–	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ refresh cycle)	t_{CHR}	10	–	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	–	ns	

- Fast page mode cycle

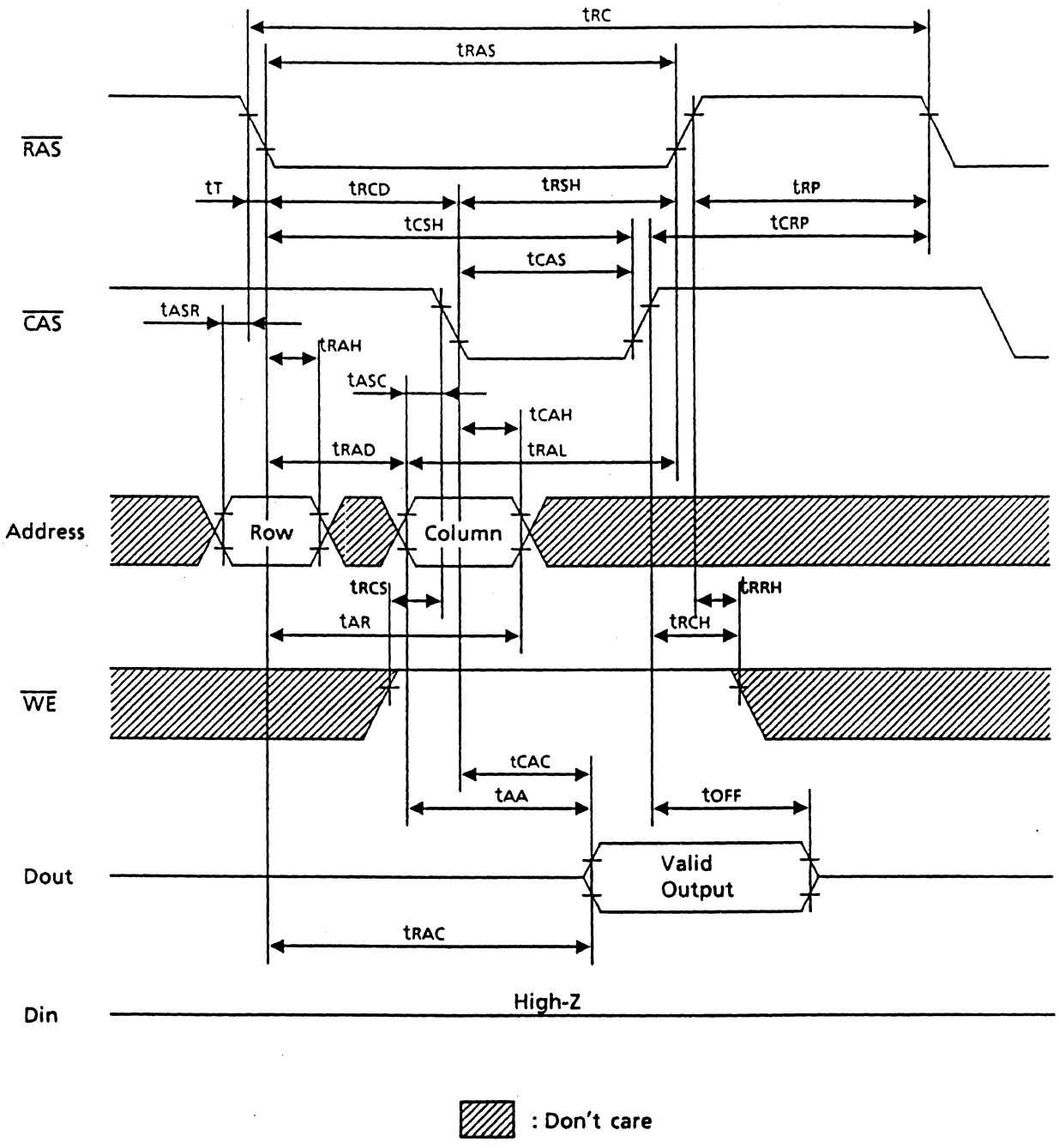
Parameter	Symbol	60ns		Unit	Note
		Min.	Max.		
Fast page mode cycle time	t_{PC}	40	–	ns	
Fast page mode $\overline{CAS}$ precharge time	t_{CP}	10	–	ns	
Fast page mode $\overline{RAS}$ pulse width	t_{RASC}	–	100000	ns	13
Access time from $\overline{CAS}$ precharge	t_{ACP}	–	35	ns	14
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35	–	ns	

Notes

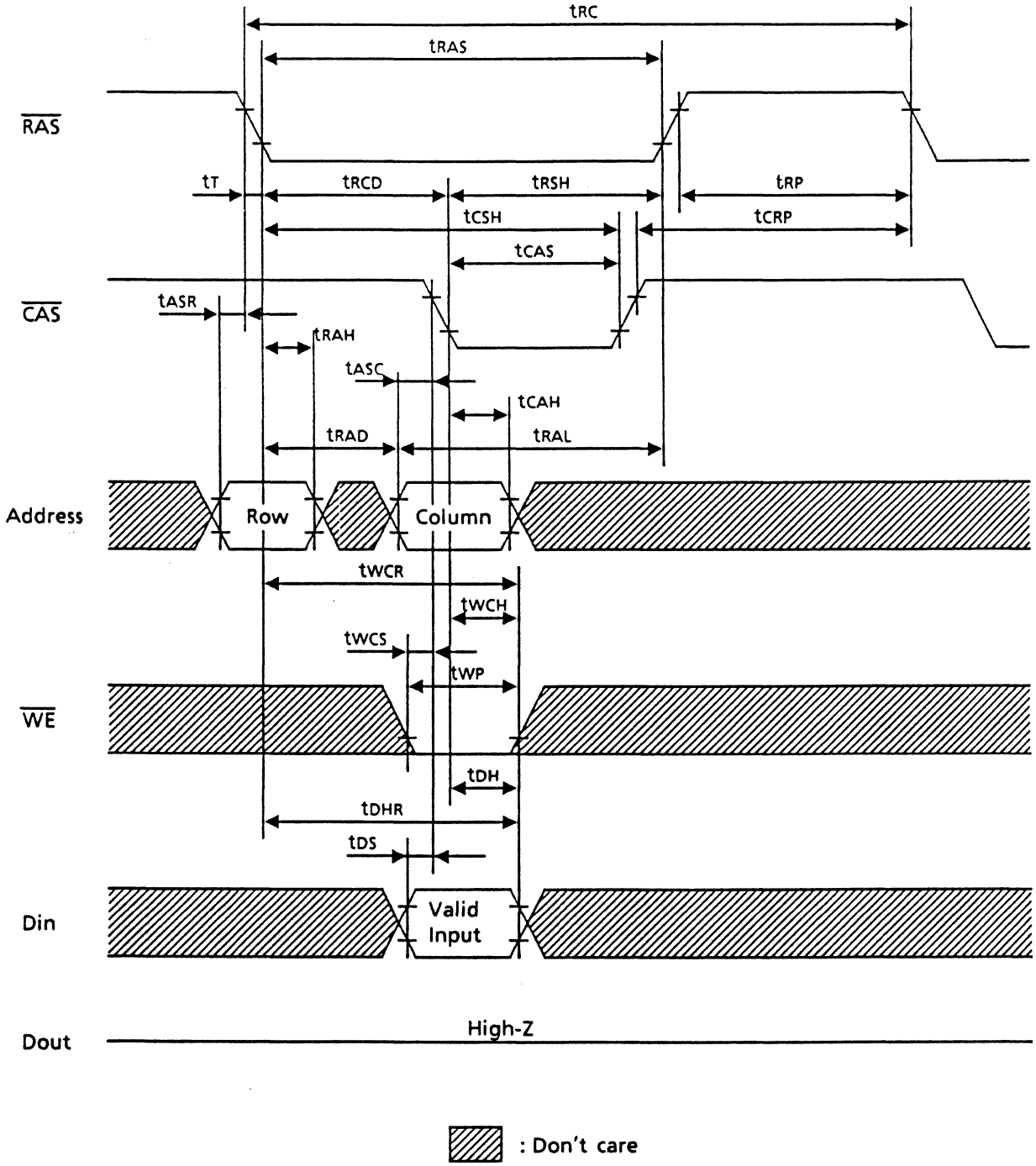
1. AC measurements assume $t_T = 5$ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max) and $t_{RAD} \leqq t_{RAD}$ (max).If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max), $t_{RAD} \leqq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leqq t_{RCD}$ (max), $t_{RAD} \geqq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geqq t_{WCS}$ (min))
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle.
12. An initial pause of 100μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh cycle or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle).
13. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
15. t_{REF} defines is 1,024 refresh cycles.

■ Timing waveform

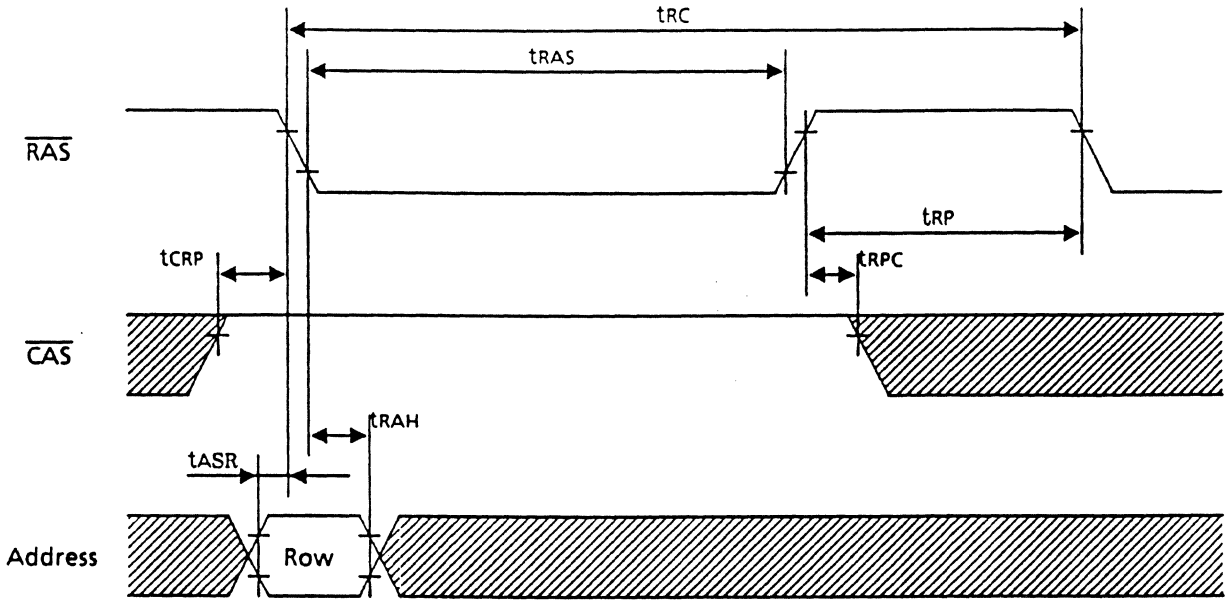
Read cycle



Early Write Cycle

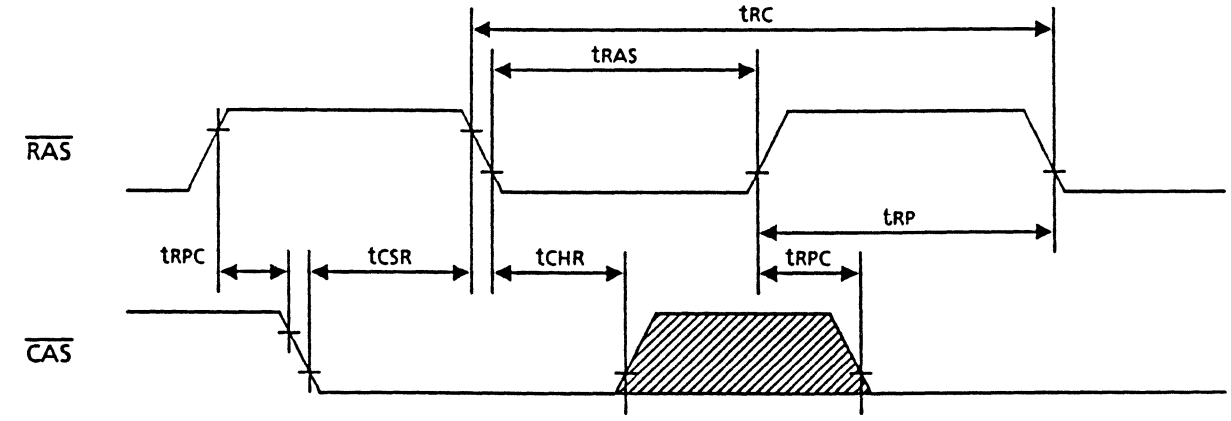


$\overline{RAS}$ Only Refresh Cycle



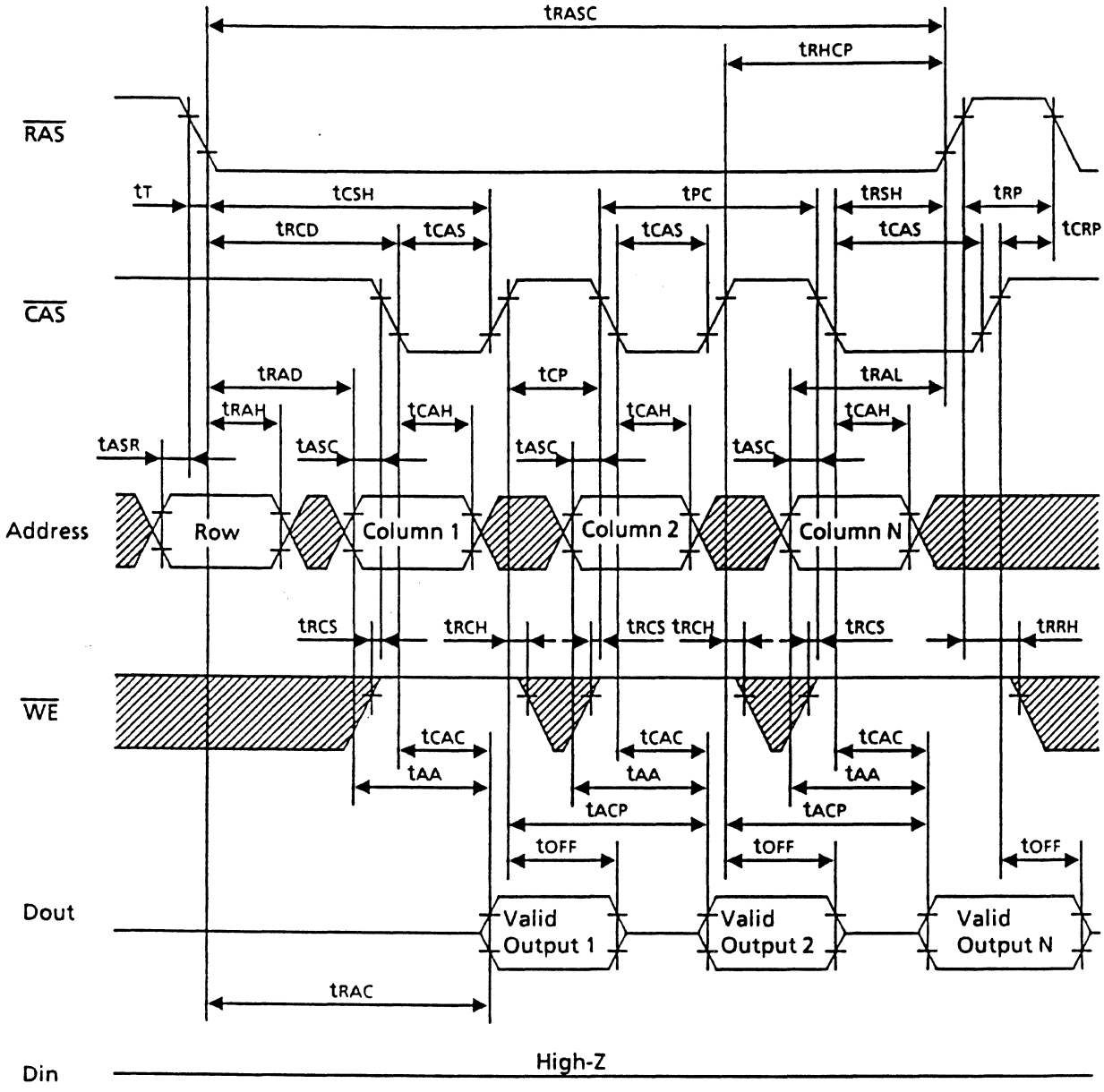
1 $\overline{WE}$: Don't care
2 ▨ : Don't care

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

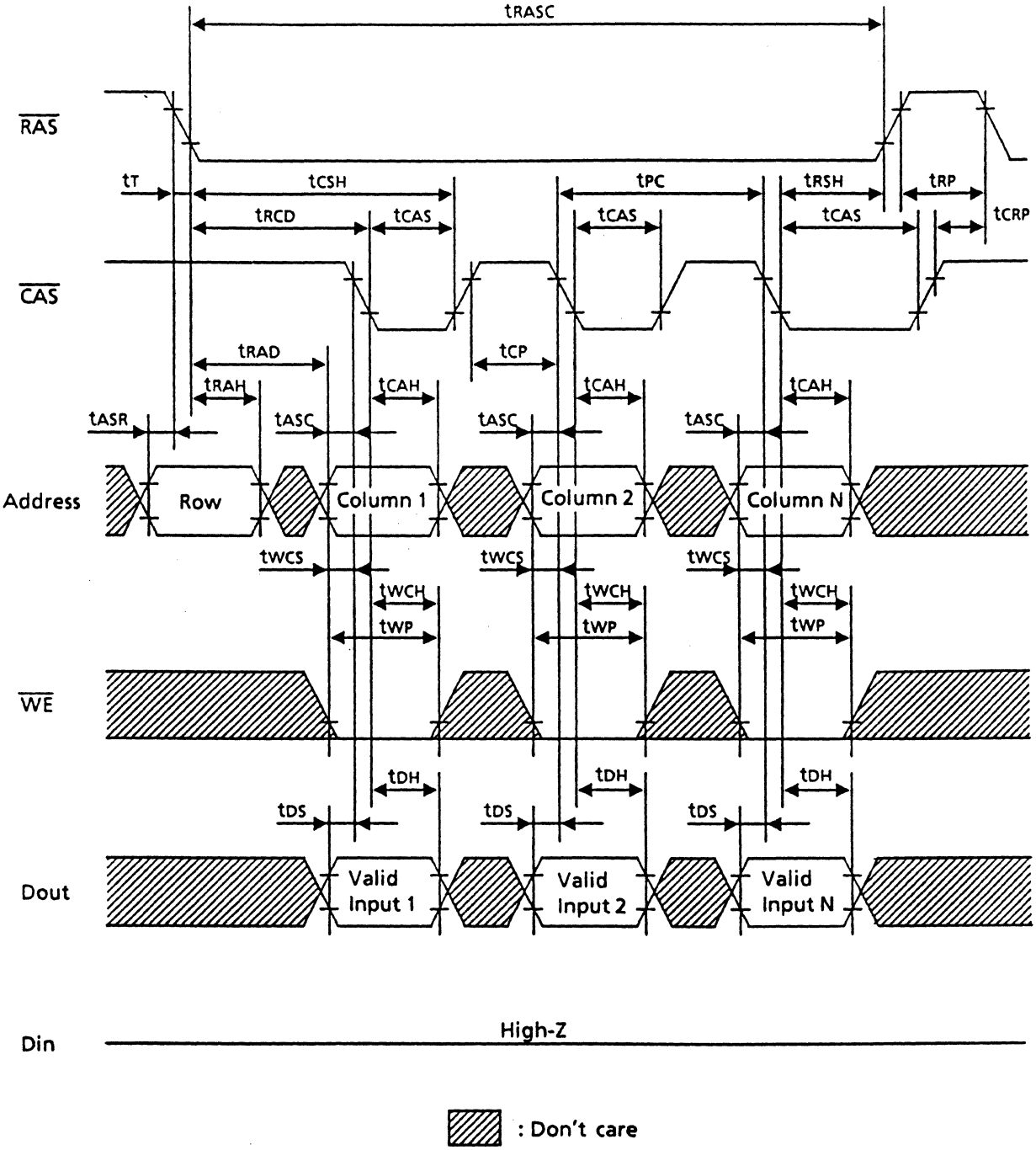


1 Address, Din : Don't care
2 Dout: High-Z
3 ▨ : Don't care
4 $\overline{WE}$ = VIH

Fast Page Mode Read Cycle



Fast Page Mode Early Write Cycle



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HITACHI

■ Revision Record

Rev.	Date	Content of Modification	Drawn by	Approved by
0	Dec,02,'91	Initial issue	T,Sugano	K,Inoue
1	Dec,12,'91	Sheet 3. Add a pull up resistor. Add $\overline{RAS1}$ and $\overline{RAS3}$ signal. Sheet 6. Changed Icc1 Spec. 900mA → 990mA	T,Sugano	K,Inoue
2	Dec,25,'91	Sheet 1. Changed part name HB56D133SU → HB56A133SU	T,Sugano	K,Inoue
3	Mar,03,'92	Sheet 9. Changed Note 12 (any combination of cycle containing .....) ↓ ($\overline{RAS}$-only refresh cycle or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle)	T. Sugano	K. Inoue

DRAM Specifications (16 MB)

On the next few pages are the SPARCclassic Engine 16 MB DRAM mechanical drawings and specifications. Use the drawings to determine the product size and shape.

DISCLAIMER: Sun Microsystems does not endorse the product as defined in the following specification. The specification is provided for information purposes only.

DISCLAIMER: The manufacturer of the product specified in the next few pages does not accept any implied warranty other than is provide with the product itself under their own purchasing agreements.

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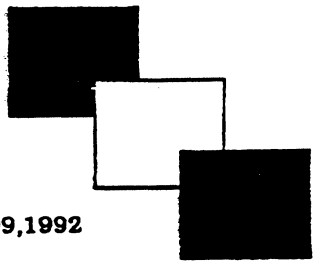
NEW PRODUCT

Sun Micro

HB56K433SU - 6

4,194,304-Word×33-Bit High Density Dynamic RAM Module



- Preliminary -

HITACHI

Rev.0
Mar,09,1992

Description

HB56K433SU is a 4M×33 dynamic RAM module, mounted 9 pieces of 16Mbit DRAM (HM5116400J) sealed in SOJ package .

An outline of the HB56K433SU is 72-pin single in-line package. Therefore, HB56K433SU makes high density mounting possible without surface mount technology. HB56K433SU provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ .

■ Feature

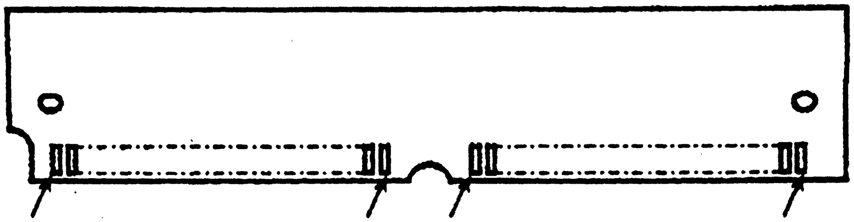
- 72-pin single in-line package
  - Lead pitch 1.27mm
- Single 5V (± 5%) supply
- High speed
  - Access time ..... 60ns (max)
- Low power dissipation
  - Active mode ..... 3.78W (max)
  - Standby mode ..... 94.5mW(max)
- Fast page mode capability
- 4,096refresh cycle / 64ms
- 2 variations of refresh
  - $\overline{RAS}$ only refresh
  - $\overline{CAS}$ before $\overline{RAS}$ refresh
- TTL compatible

■ Ordring Information

Part No.	Access time	Package	Contact pads
HB56K433SU - 6	60ns	72-pin single in-line package Socket type	Solder coat

Preliminary : This document contains information on a new product. Specifications and information contained herein are subject to change without notice.
新製品のデータシートです。掲載内容は,予告なく変更,廃止されることがあります。

■ Pin Out



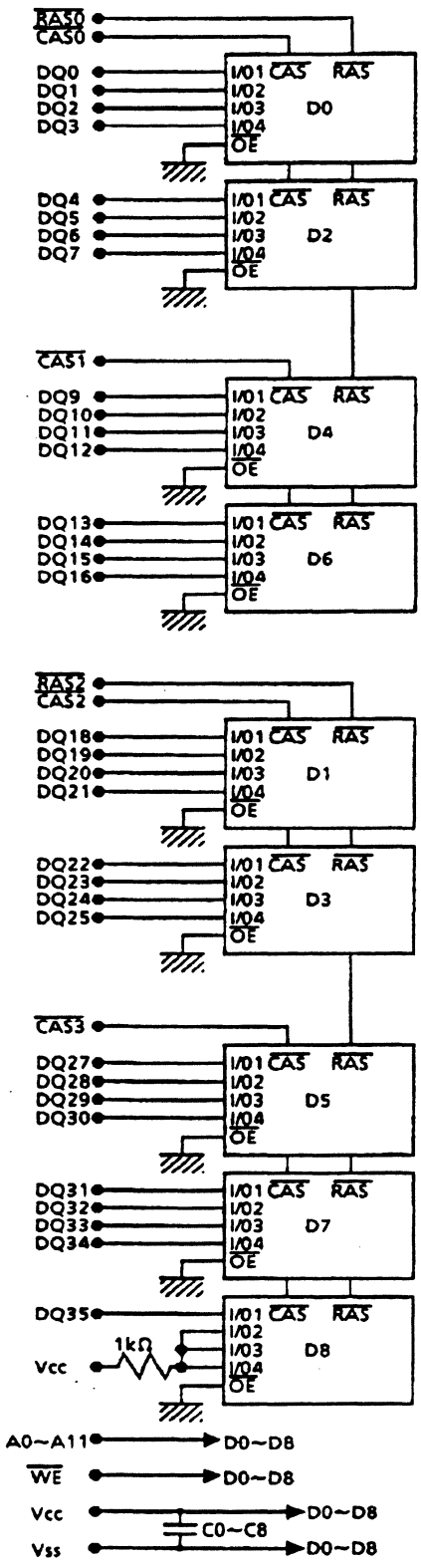
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	19	A10	37	NC	55	DQ12
2	DQ0	20	DQ4	38	DQ35	56	DQ30
3	DQ18	21	DQ22	39	V_{SS}	57	DQ13
4	DQ1	22	DQ5	40	$\overline{CAS0}$	58	DQ31
5	DQ19	23	DQ23	41	$\overline{CAS2}$	59	V_{CC}
6	DQ2	24	DQ6	42	$\overline{CAS3}$	60	DQ32
7	DQ20	25	DQ24	43	$\overline{CAS1}$	61	DQ14
8	DQ3	26	DQ7	44	$\overline{RAS0}$	62	DQ33
9	DQ21	27	DQ25	45	NC	63	DQ15
10	V_{CC}	28	A7	46	NC	64	DQ34
11	NC	29	A11	47	$\overline{WE}$	65	DQ16
12	A0	30	V_{CC}	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	T.B.D. *
14	A2	32	A9	50	DQ27	68	T.B.D. *
15	A3	33	NC	51	DQ10	69	T.B.D. *
16	A4	34	$\overline{RAS2}$	52	DQ28	70	T.B.D. *
17	A5	35	NC	53	DQ11	71	NC
18	A6	36	NC	54	DQ29	72	V_{SS}

* Presense detect pin using jumper-chip.

■ Pin Description

Pin Name	Function	Pin Name	Function
A0 – A11	Address Input : A0 – A11 Row Address : A0 – A11 Column Address : A0 – A9 Refresh Address : A0 – A11	$\overline{CAS0}$ – $\overline{CAS3}$	Column Address Strobe
		$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
		$\overline{WE}$	Read / Write Enable
DQ0 – DQ7 DQ9 – DQ16 DQ18 – DQ25 DQ27 – DQ35	Data-in / Data-out	V_{CC}	Power Supply (+5V)
		V_{SS}	Ground
		NC	No connection

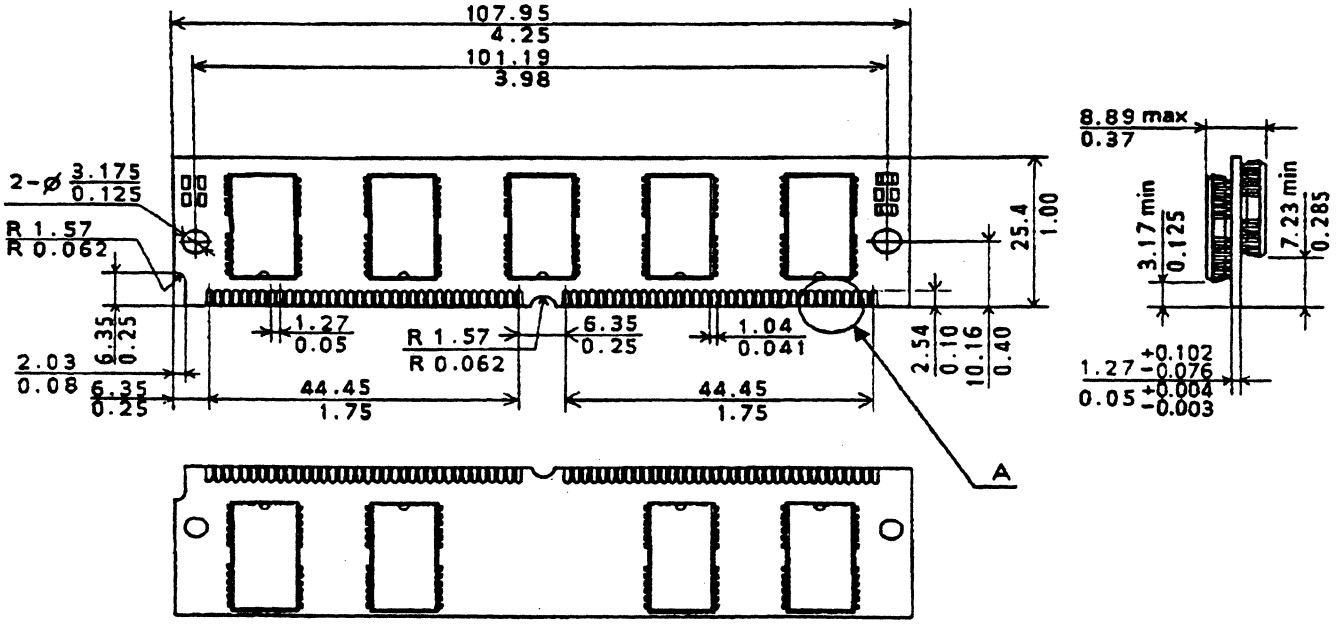
■ Block Diagram



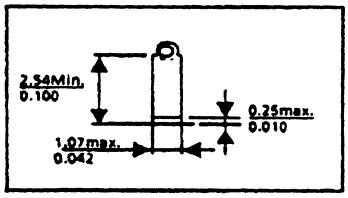
D0~D8 : HM5116400J

■ Physical Outline

Unit : mm / inch



Detail A



■ Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	(Input)	V_{IN}	−1.0 to +7.0	V
	(Output)	V_{OUT}	−1.0 to +7.0	V
Supply voltage relative to V_{SS}		V_{CC}	−1.0 to +7.0	V
Short circuit output current		I_{out}	50	mA
Power dissipation		P_T	9	W
Operating temperature		T_{opr}	0 to +70	°C
Storage temperature		T_{stg}	−55 to +125	°C

■ Electrical Characteristics

☆ Recommended DC Operating Conditions (T_a = 0 to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	−1.0	—	0.8	V	1

Note : 1. All voltage referenced to V_{SS}

☆ DC Electrical Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 5%, V_{SS} = 0V)

Parameter	Symbol	60ns		Unit	Test Condition	Note
		Min.	Max.			
Operating current	I_{CC1}	–	720	mA	t_{RC} = min	1,2
Standby current	I_{CC2}	–	18	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{OUT} = High-Z	
		–	9	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≧ V_{CC} – 0.2V D_{OUT} = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	–	720	mA	t_{RC} = min	2
Standby current	I_{CC5}	–	45	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{OUT} = enable	1
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC6}	–	720	mA	t_{RC} = min	
Page mode current	I_{CC7}	–	630	mA	t_{PC} = min	1,3
Input leakage current	I_{LI}	–10	10	μA	0V ≦ V_{IN} ≦ 7V	
Output leakage current	I_{LO}	–10	10	μA	0V ≦ V_{OUT} ≦ 7V D_{OUT} = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	V	High I_{OUT} = –5mA	
Output low voltage	V_{OL}	0	0.4	V	Low I_{OUT} = 4.2mA	

Note : 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.

2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.

3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

☆ Capacitance ($Ta = 25°C$, $V_{CC} = 5V \pm 5\%$)

Parameter	Symbol	60ns		Unit	Note
		Typ.	Max.		
Input capacitance (Address)	C_{I1}	–	73	pF	1
Input capacitance ($\overline{WE}$)	C_{I2}	–	83	pF	1
Input capacitance ($\overline{RAS}$)	C_{I3}	–	50	pF	1
Input capacitance ($\overline{CAS}$)	C_{I4}	–	36	pF	1
Output capacitance (DQ0–7, 9–16, 18–25, 27–35)	$C_{I/O}$	–	17	pF	1, 2

Note : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS} = V_{IH}$ to disable D_{OUT}.

☆ AC Characteristics ($Ta = 0$ to $70°C$, $V_{CC} = 5V \pm 5\%$, $V_{SS} = 0V$) 1), 2)

- Read , Write and Refresh Cycle (Common parameters)

Parameter	Symbol	Min.	Max.	Unit	Note
Ramdom read or write cycle time	t_{RC}	110	–	ns	
$\overline{RAS}$ precharge time	t_{RP}	40	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10000	ns	
Row address setup time	t_{ASR}	0	–	ns	
Row address hold time	t_{RAH}	10	–	ns	
Column address setup time	t_{ASC}	0	–	ns	
Column address hold time	t_{CAH}	15	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	ns	3
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	ns	4
$\overline{RAS}$ hold time	t_{RSH}	15	–	ns	
$\overline{CAS}$ hold time	t_{CSH}	60	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	ns	
Transition time (rise and fall)	t_T	3	30	ns	5
Refresh period	t_{REF}	–	64	ms	17

- **Read Cycle**

Parameter	Symbol	Min.	Max.	Unit	Note
Access time from $\overline{RAS}$	t_{RAC}	–	60	ns	6,7,16
Access time from $\overline{CAS}$	t_{CAC}	–	15	ns	7,8,15,16
Access time from address	t_{AA}	–	30	ns	7,9,15,16
Read command setup time	t_{RCS}	0	–	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	–	ns	10
Read command hold time to $\overline{RAS}$	t_{RRH}	5	–	ns	10
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	–	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	30	–	ns	
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0	–	ns	
Output buffer turn-off time	t_{OFF}	0	15	ns	11

- **Write Cycle**

Parameter	Symbol	Min.	Max.	Unit	Note
Write command setup time	t_{WCS}	0	–	ns	12
Write command hold time	t_{WCH}	15	–	ns	
Write command pulse width	t_{WP}	15	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	–	ns	
Data-in setup time	t_{DS}	0	–	ns	13
Data-in hold time	t_{DH}	15	–	ns	13

- Refresh Cycle

Parameter	Symbol	Min.	Max.	Unit	Note
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	10	–	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	20	–	ns	
$\overline{WE}$ setup time (CBR refresh cycle)	t_{WRP}	10	–	ns	
$\overline{WE}$ hold time (CBR refresh cycle)	t_{WRH}	10	–	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	0	–	ns	

- Fast Page Mode Cycle

Parameter	Symbol	Min.	Max.	Unit	Note
Fast page mode cycle time	t_{PC}	40	–	ns	
Fast page mode $\overline{CAS}$ precharge time	t_{CP}	10	–	ns	
Fast page mode $\overline{RAS}$ pulse width	t_{RASP}	–	100000	ns	14
Access time from $\overline{CAS}$ precharge	t_{CPA}	–	35	ns	7,15,16
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{CPRH}	35	–	ns	

- Test Mode Cycle

Parameter	Symbol	Min.	Max.	Unit	Note
Test mode $\overline{WE}$ setup time	t_{WTS}	10	–	ns	
Test mode $\overline{WE}$ hold time	t_{WTH}	10	–	ns	

- Counter Test Cycle

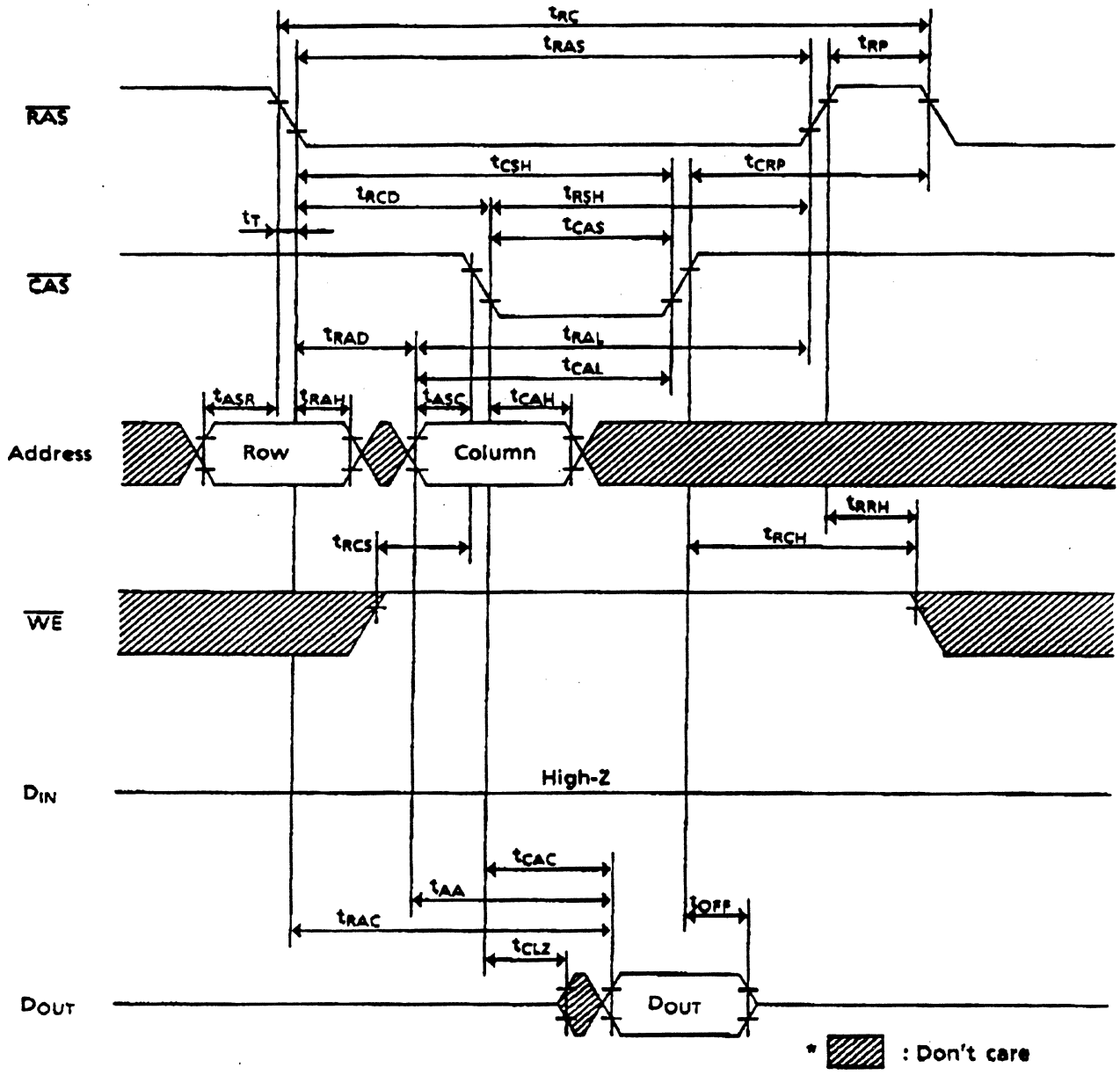
Parameter	Symbol	Min.	Max.	Unit	Note
$\overline{CAS}$ precharge time in counter test cycle	t_{CPT}	40	–	ns	

Notes

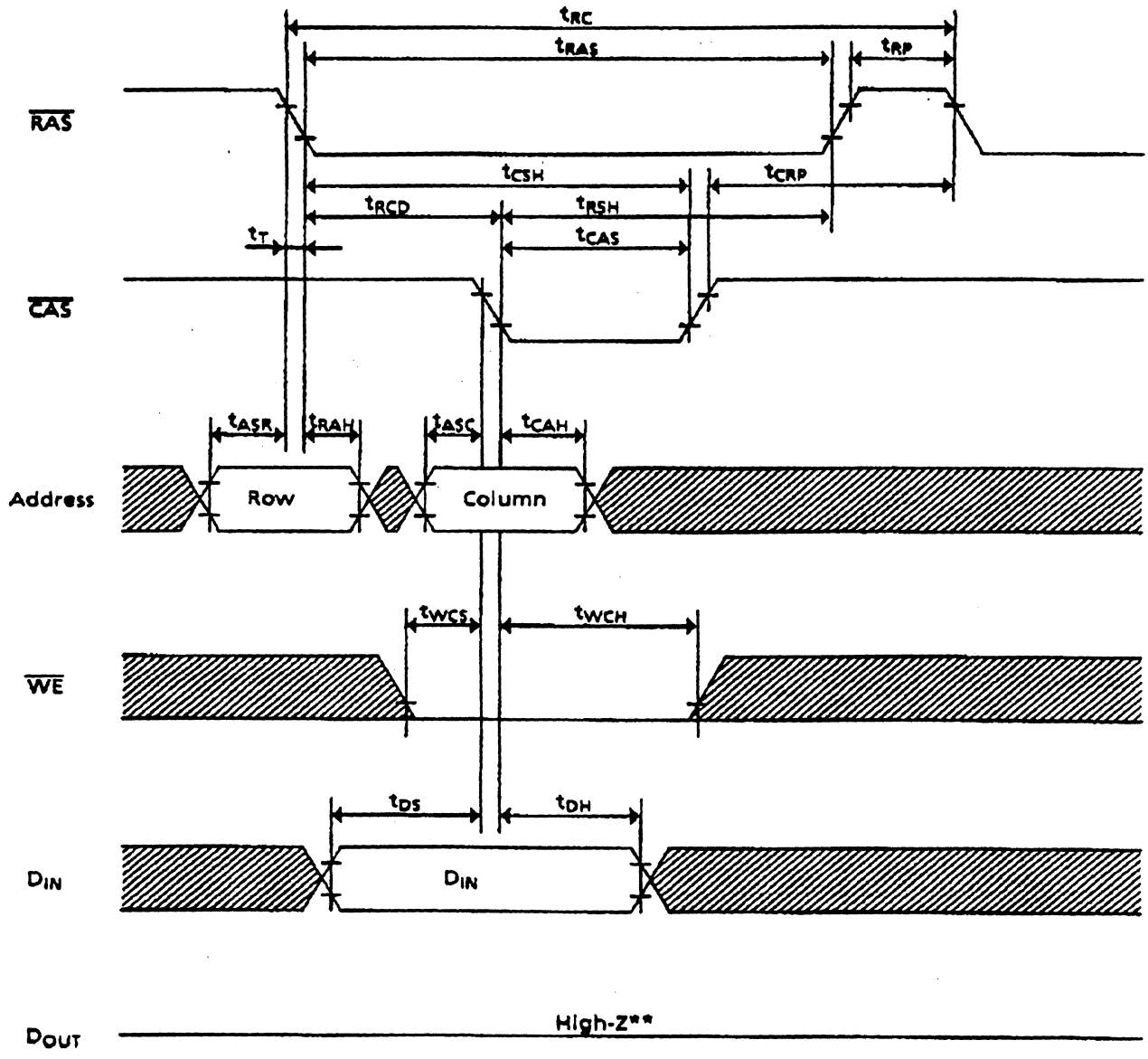
1. AC measurements assume $t_T = 5ns$.
2. An initial pause of 200us is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$-only refresh or $\overline{CAS}$-before-$\overline{RAS}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
3. Operation with the t_{RCD}(max) limit insures that t_{RAC}(max) can be met, t_{RCD}(max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
4. Operation with the t_{RAD}(max) limit insures that t_{RAC}(max) can be met, t_{RAD}(max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled exclusively by t_{AA}.
5. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL}(max).
6. Assumes that $t_{RCD} \leq t_{RCD}$(max) and $t_{RAD} \leq t_{RAD}$(max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
7. Measured with a load circuit equivalent to 2TTL loads and 100pF.
8. Assumes that $t_{RCD} \geq t_{RCD}$(max), $t_{RAD} \leq t_{RAD}$(max).
9. Assumes that $t_{RCD} \leq t_{RCD}$(max), $t_{RAD} \geq t_{RAD}$(max).
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
11. t_{OFF}(max) is define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Early write cycle only. ($t_{WCS} \geq t_{WCS}$(min.))
13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles.
14. t_{RASP} defines $\overline{RAS}$ pulse width in fast page mode cycles.
15. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{CPA}.
16. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} and t_{CPA} is delayed for 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
17. t_{REF} is determined by 4,096 refresh cycles.

■ Timing Waveform

Read Cycle



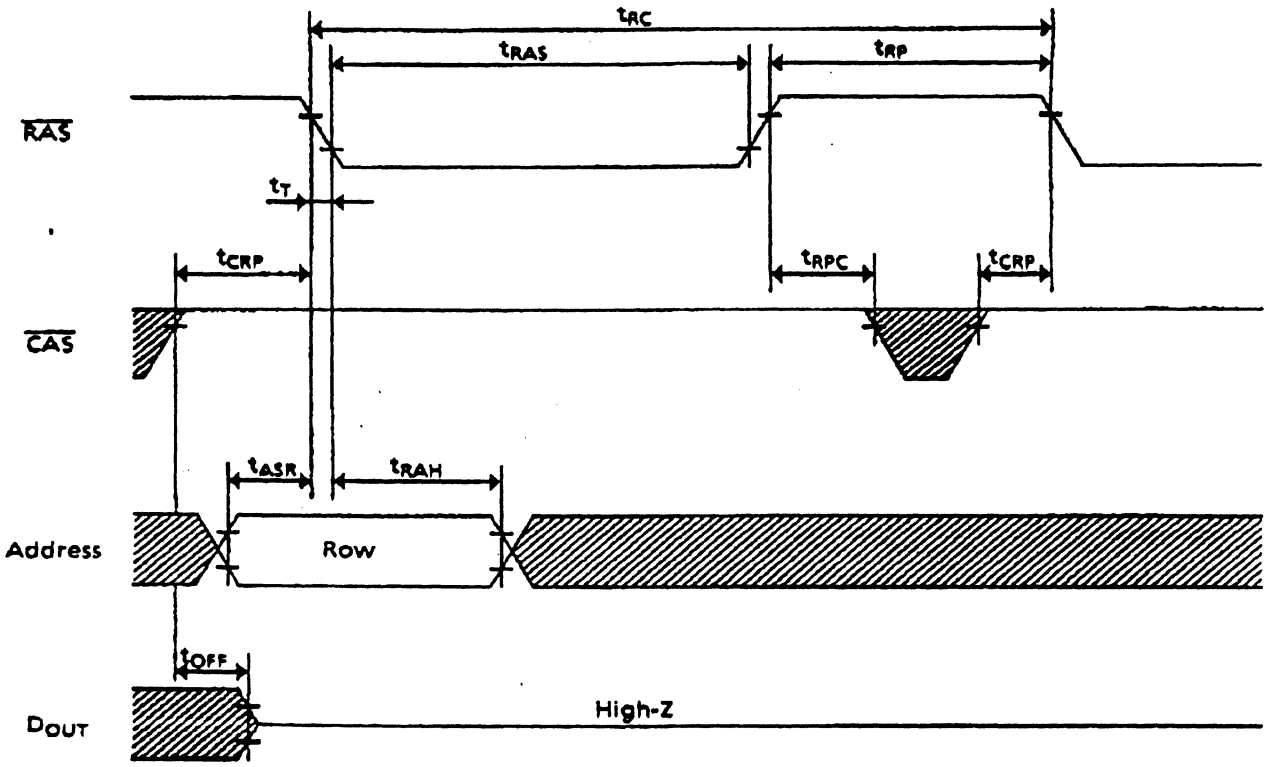
Early write cycle



* : Don't care

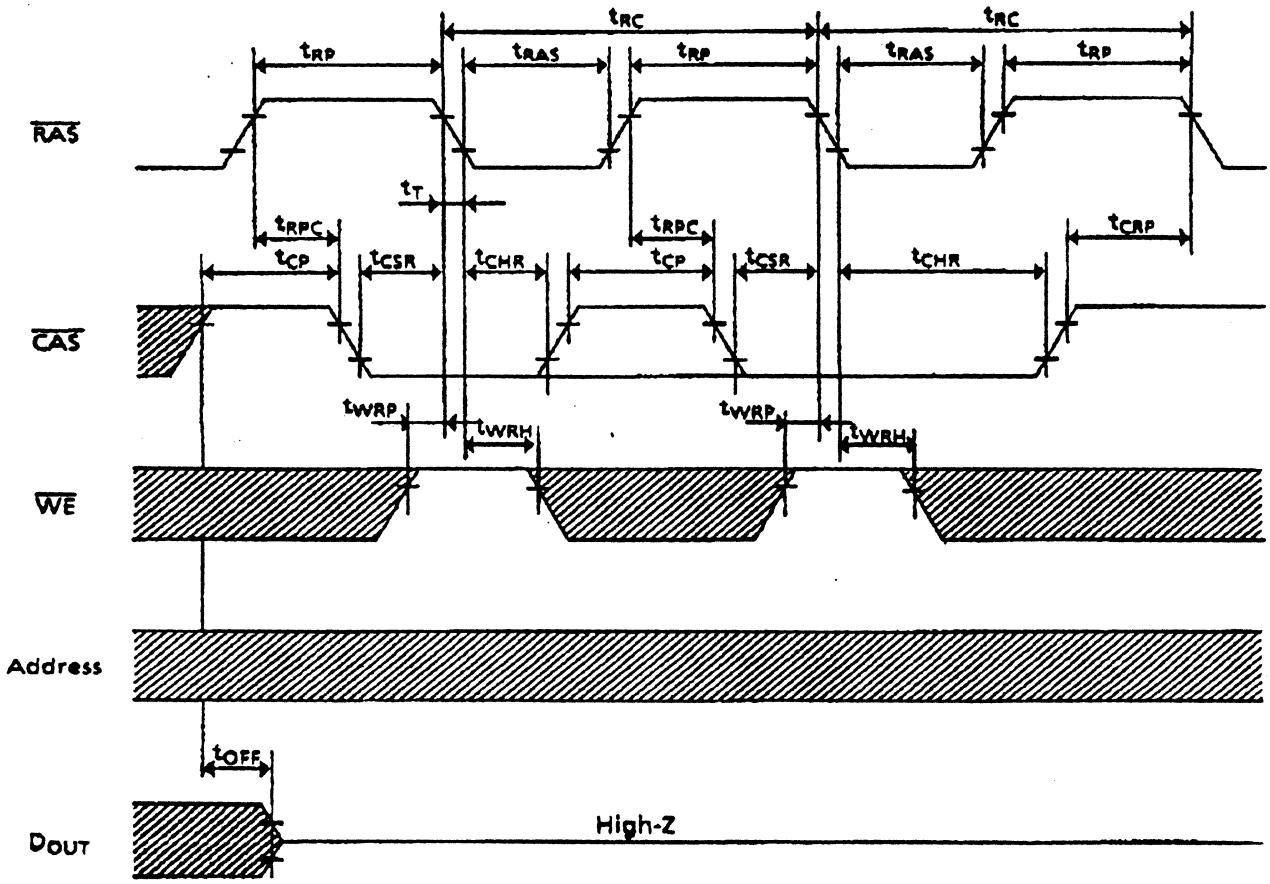
** $t_{WCS} \geq t_{WCS}$ (min)

$\overline{RAS}$-Only Refresh Cycle



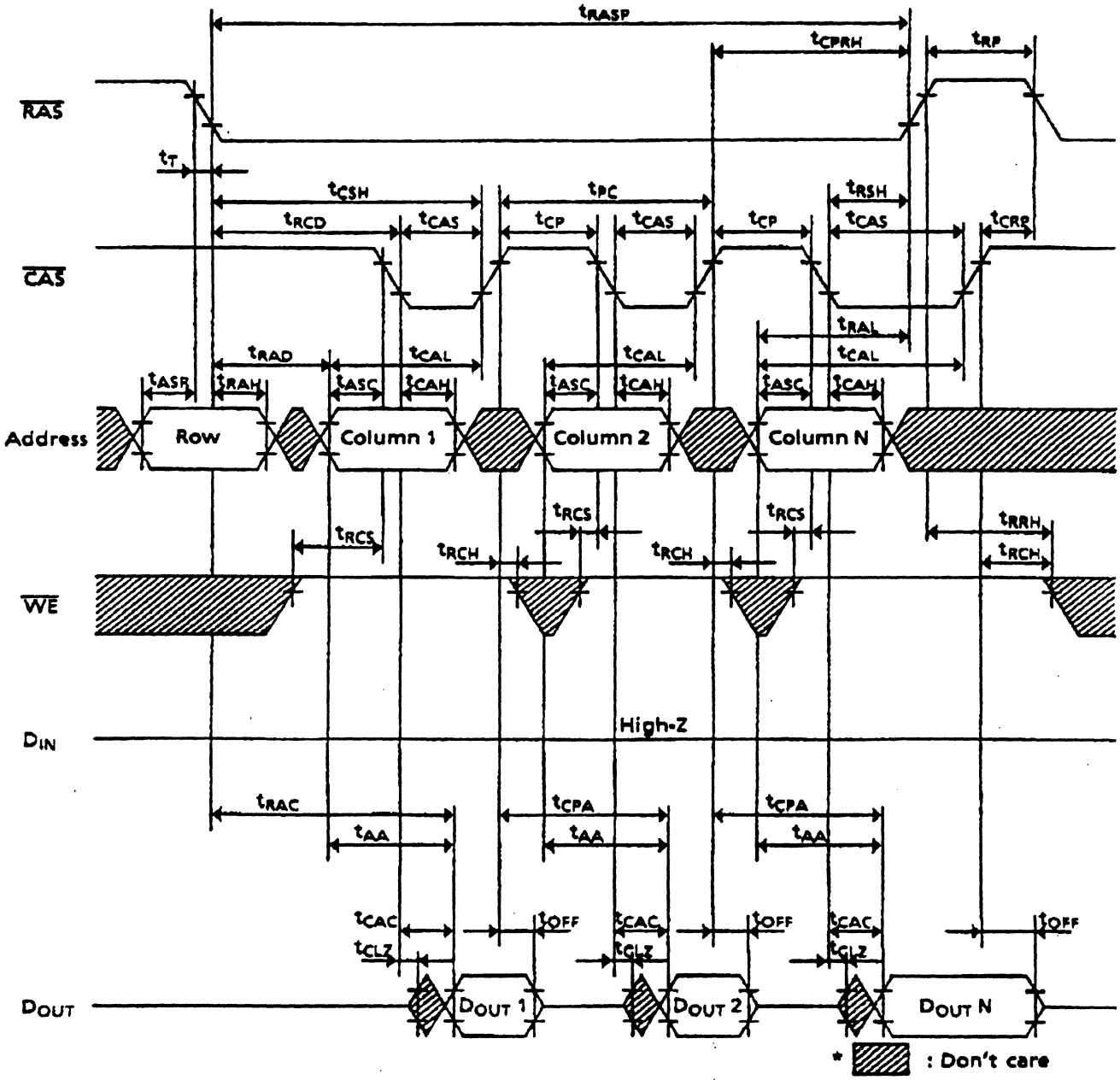
* $\overline{WE}$: Don't care
** ▨ : Don't care
*** Refresh address : A0 – A11 (RA0 – RA11)

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle

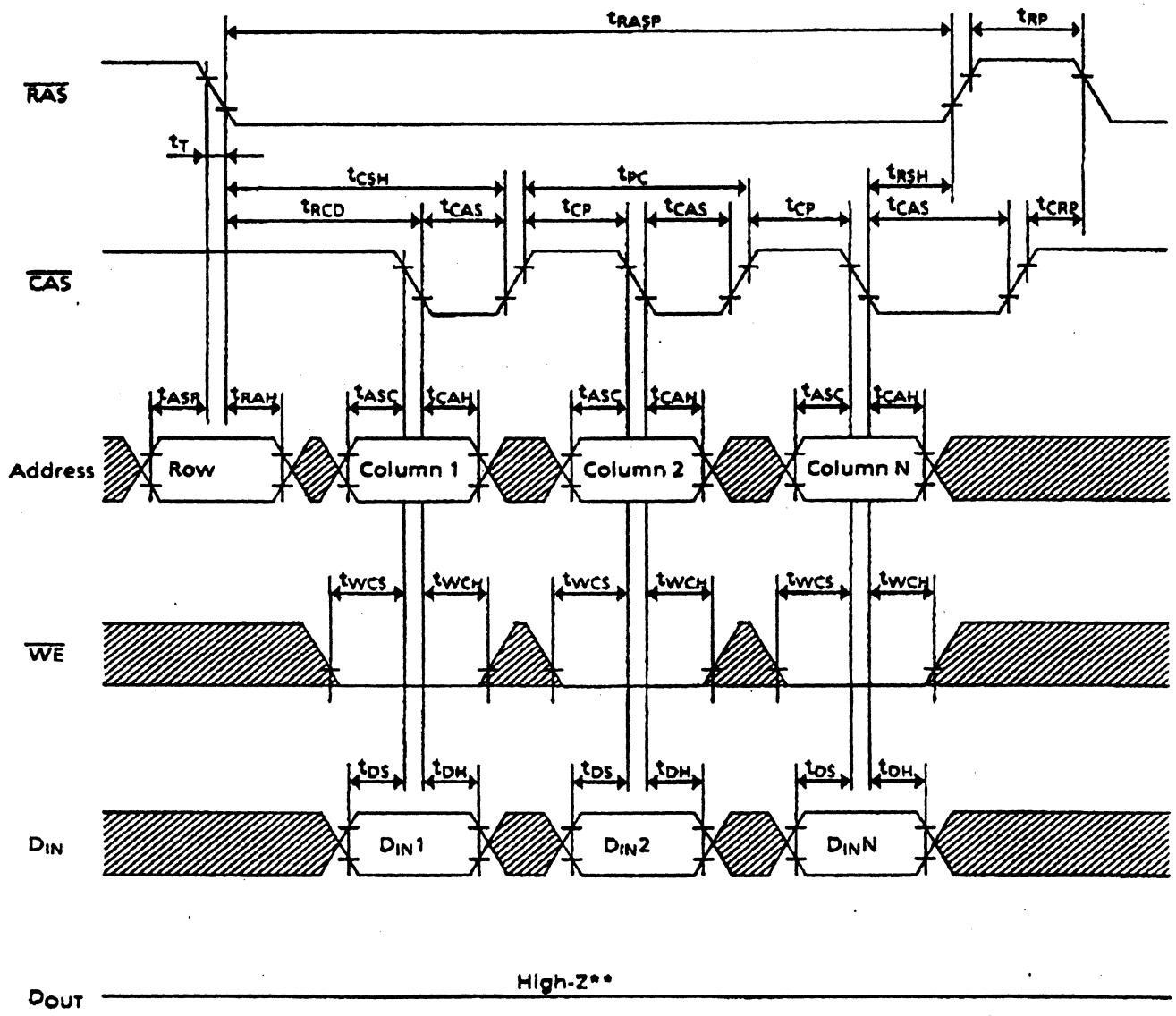


* ▨ : Don't care

Fast Page Mode Read Cycle



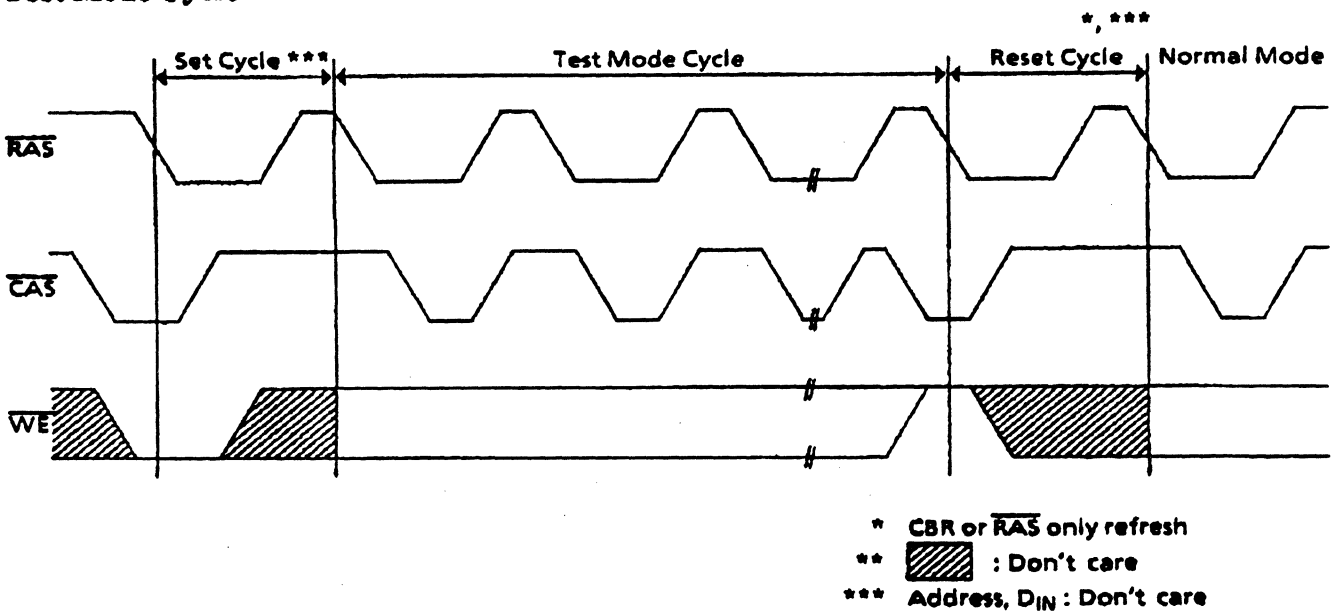
Fast Page Mode Early Write Cycle



* ▨ : Don't care

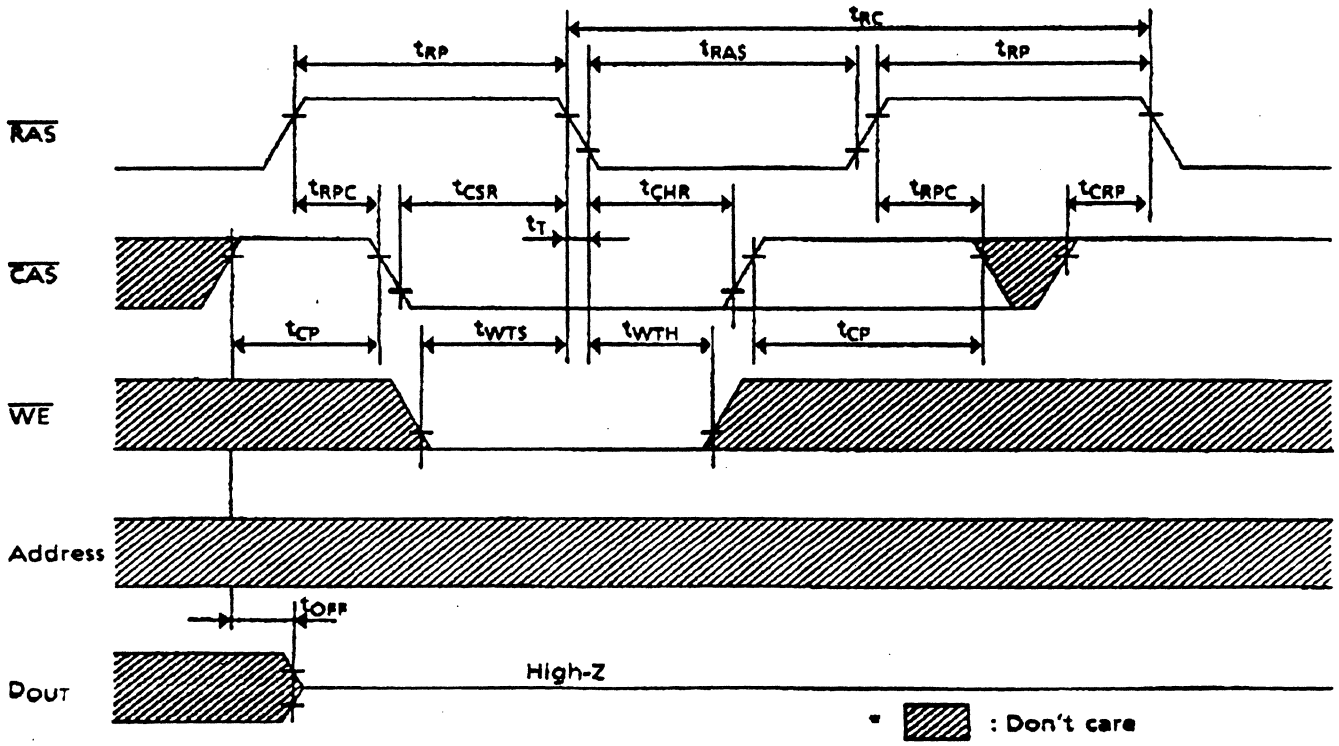
** $t_{WCS} \geq t_{WCS}$ (min)

Test Mode Cycle



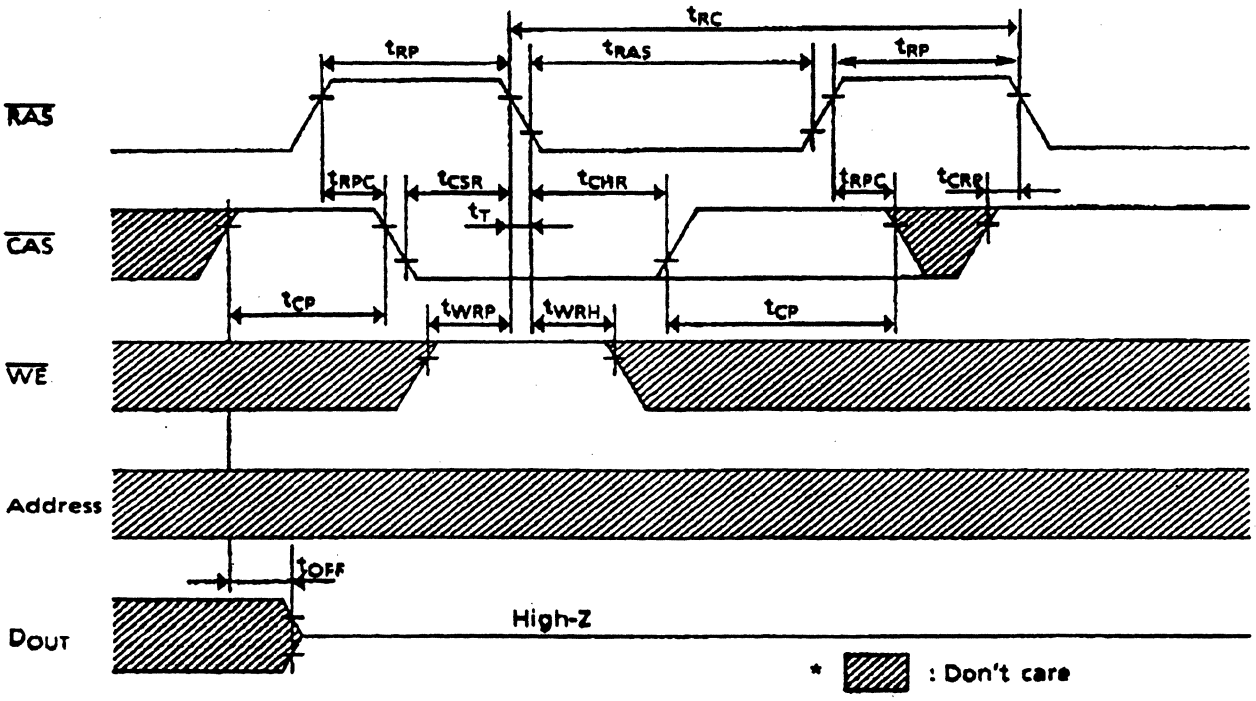
* CBR or $\overline{RAS}$ only refresh
** ▨ : Don't care
*** Address, D_{IN} : Don't care

Test Mode Set Cycle

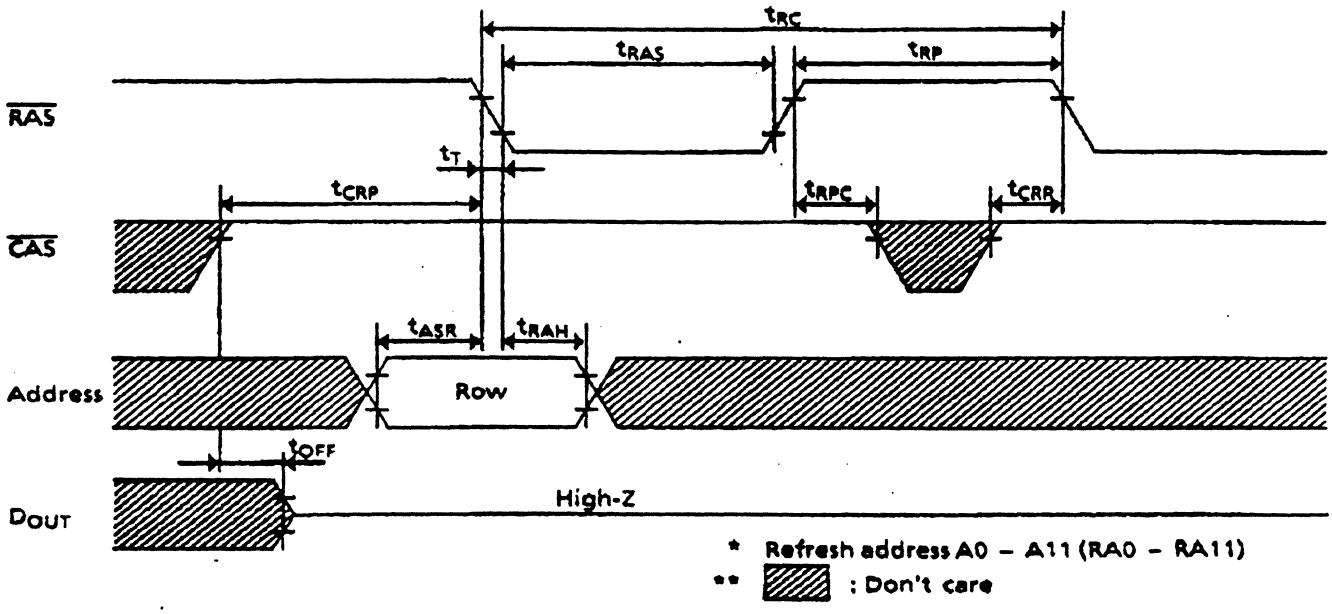


Test Mode Reset Cycle

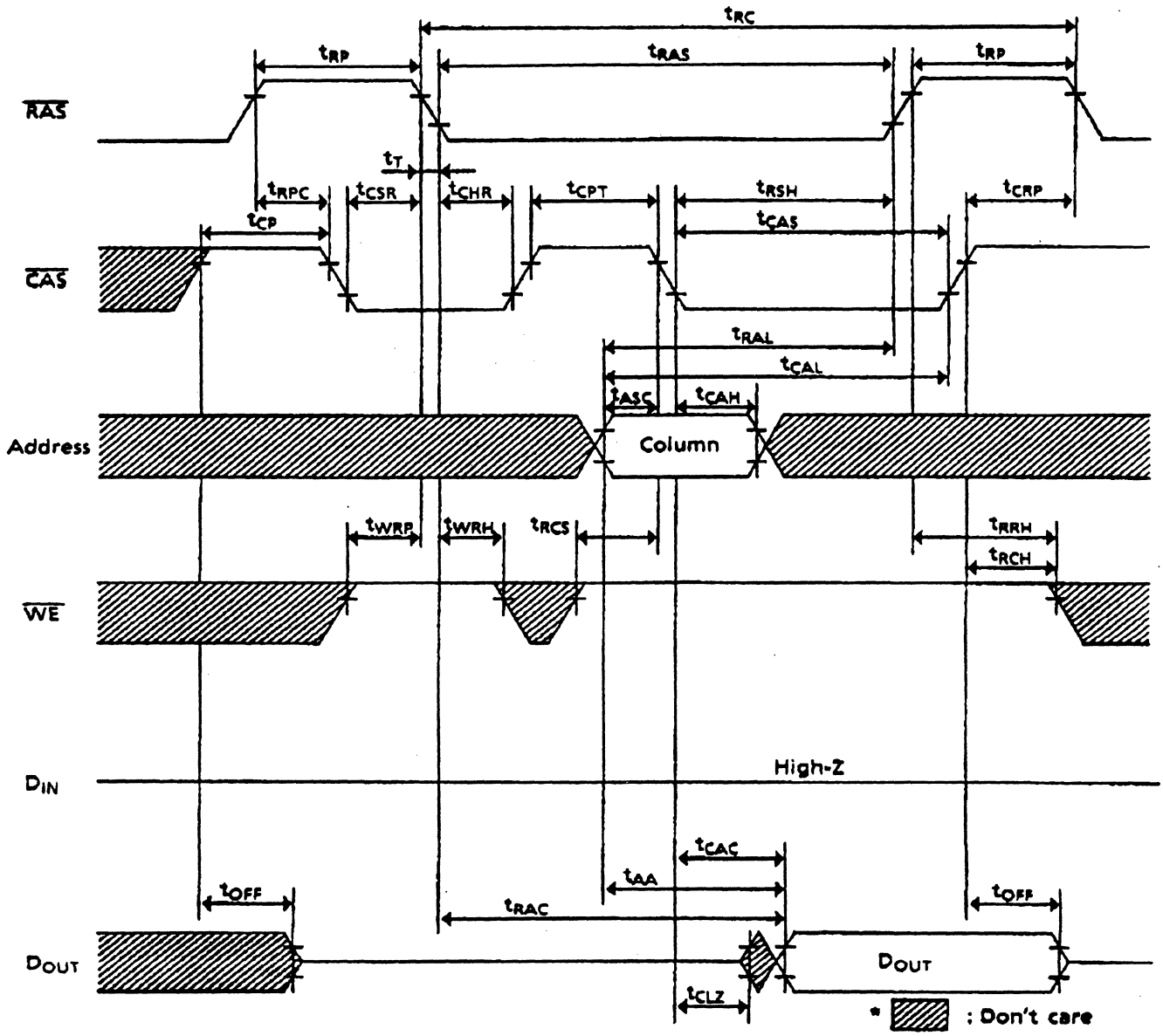
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle



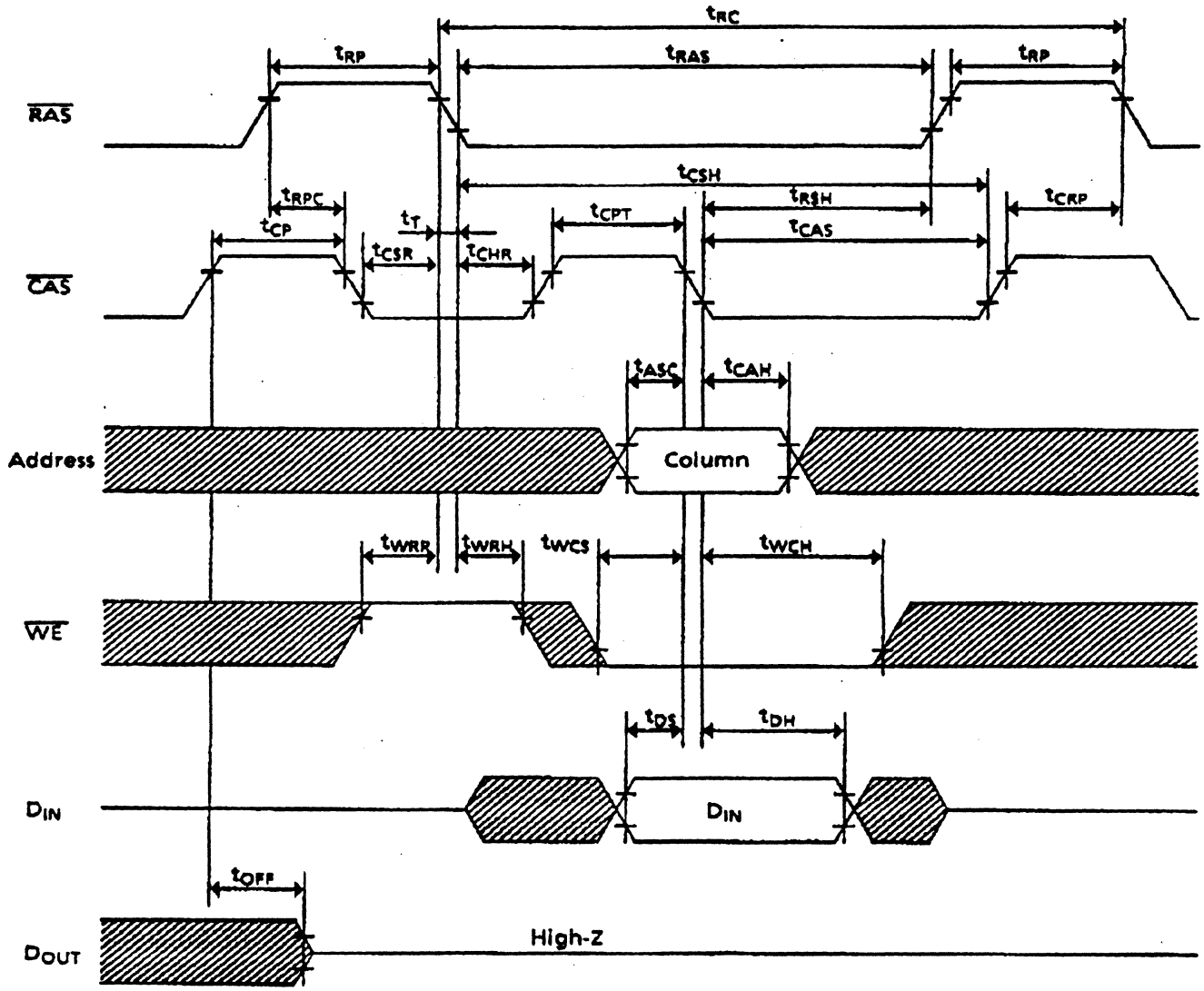
$\overline{RAS}$-Only Refresh Cycle



CAS-Before-RAS Refresh Counter Check Cycle (Read)



$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Check Cycle (Write)



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HITACHI

■ Revision Record

Rev.	Data	Content of Modification	Drawn by	Approved by
0	Mar.09,'92	Initial issue	T. Sugano	K. Inoue

160-Pin I/O Connector Specifications

If you are going to design your own I/O board to use with the SPARCclassic Engine, use the following 160-pin I/O connector specifications provided in the next few pages to purchase the appropriate female to match the male edge-connector on the SPARCclassic Engine.

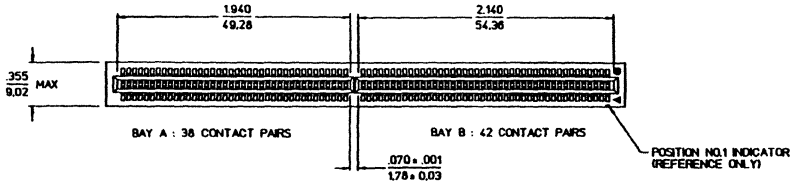
DISCLAIMER: Sun Microsystems does not endorse the product as defined in the following specification. The specification is provided for information purposes only.

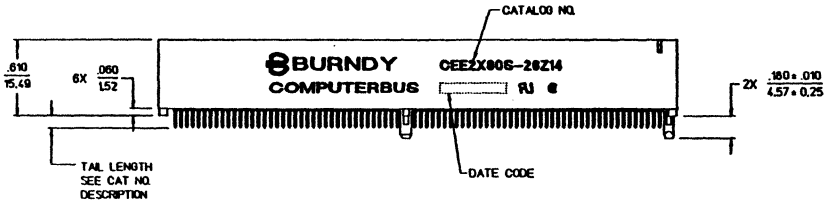
DISCLAIMER: The manufacturer of the product specified in the next few pages does not accept any implied warranty other than is provide with the product itself under their own purchasing agreements.

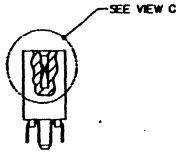
CATALOG NUMBER DESCRIPTION

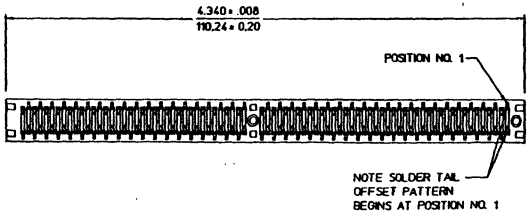
CE E 2X 80 S - 26 Z14

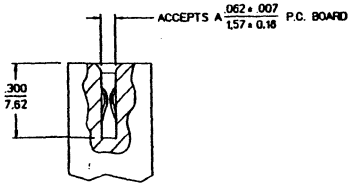
- CE — CONNECTOR SERIES EDGE CARD
- E — CONTACT SPACING E=.050 [1.27] PITCH
- 2X — NUMBER OF ROWS
- 80 — NUMBER OF CONTACTS PER ROW
- S — TERMINATION STYLE S= SOLDER TAIL
- 26 — DESIGN VARIATION 26= .100 x.010 [2.54 x0.25] TAIL LENGTH AND SOLID END HOUSING
- Z14 — PLATING DESIGNATION











VIEW C
SCALE 4 : 1

NOTES: UNLESS OTHERWISE SPECIFIED,

1. INTERPRET THIS DRAWING IN ACCORDANCE WITH ANSI Y14.5M - 1982.
2. SEE SHEETS 2 AND 4 FOR RECOMMENDED MATING P.C. BOARD CONTACT PAD AND BACKPLANE LAYOUTS.
3. MATING P.C. BOARD MATERIAL:
   P.C. BOARD: FR-4 WITH 1 oz. [28.35 GRAMS] MIN COPPER PADS

   PAD PLATING: 30 MICROINCHES [0.76 MICRONS] MIN. GOLD PER MIL-G-45204, TYPE 1, CLASS 1, GRADE C, OVER 100 MICROINCHES [2.54 MICRONS] MIN. NICKEL PER QQ-N-290.

MATERIALS:

BODY: GLASS-FILLED THERMOPLASTIC, RATED UL94V-0
COLOR- NATURAL

CONTACTS: COPPER ALLOY

CONTACT FINISH:
Z14 PLATING: GOLD FLASH OVER 40 MICROINCHES [1.02 MICRONS] MIN. PALLADIUM-NICKEL OVER 50 MICROINCHES [1.27 MICRONS] MIN. NICKEL UNDERPLATE IN CRITICAL CONTACT AREA AND 100 MICROINCHES [2.54 MICRONS] SOLDER OVER NICKEL UNDERPLATE ON SOLDER TAILS.

PERFORMANCE CHARACTERISTICS:

CONTACT RESISTANCE (LOW SIGNAL LEVEL): MIL-STD-1344, METHOD 3002-1, 30 MILLIOHMS MAXIMUM INITIAL, 10 MILLIOHMS MAXIMUM INCREASE THROUGH TESTING.

CURRENT RATING: 1 AMP, PER EACH POWER CONTACT.

CONTACT NORMAL FORCE: 1.76 OZ FORCE [0.49 NEWTONS] MIN END OF LIFE.

DURABILITY: 100 MATING CYCLES WITHOUT PHYSICAL DAMAGE OR EXCEEDING LOW LEVEL CONTACT RESISTANCE REQUIREMENT WHEN MATED WITH RECOMMENDED CARD EDGE.

INSULATION RESISTANCE: MIL-STD-202, METHOD 302, CONDITION B, 1000 MEGAOHMS MINIMUM.

OPERATING TEMPERATURE: -40°F TO 221°F [-40°C TO 105°C].

THERMAL SHOCK: MIL-STD-1344, METHOD 1003.1 -67°F TO 185°F [-55°C TO 85°C], 5 CYCLES.

CAPACITANCE: 2 PICOFARADS, MAXIMUM AT 1 MEGAHERTZ.

BOTH CONTACTS AND BODY ARE ABLE TO WITHSTAND VAPOR PHASE TEMPERATURE EXPOSURE.

MATING FORCE: MIL-STD-1344, METHOD 2013.1, 6 OZ FORCE [1.668 NEWTONS] MAXIMUM AVERAGE PER OPPOSING PAIR USING GAUGE PER MIL-STD-C-21097, EXCEPT .062[1.57] THICK, WITH 20° ANGLE.

SUPERSEDES: SKME27681 REV. 0

REFERENCE: SE93533

REV	REVISION DESCRIPTION	BY	CHKD	DATE

CAGE NO 09922 | DON641 | PC 822

COMPUTERBUS CARD EDGE CONNECTOR (SOLID ENDS)

CAT NO CEE2X80S-26Z14 | SCALE 2 : 1

DRAWN	AEW 03-20-92	APVL	DSGN YIP 04-01-92
CHECKED	VCE 03-24-92		MKT BM 04-02-92
			QC JB 04-20-92

LINEAR MEASURE: INCH / mm — INCH [mm]
THIRD ANGLE PROJECTION
- TOLERANCES - UNLESS OTHERWISE SPECIFIED

NO OF DECIMAL PLACES IN INCHES	INCH [mm]
ONE PLACE	±.1 [±2.5]
TWO PLACES	±.02 [±0.5]
THREE PLACES	±.005 [±0.13]
ANGLES	±1°

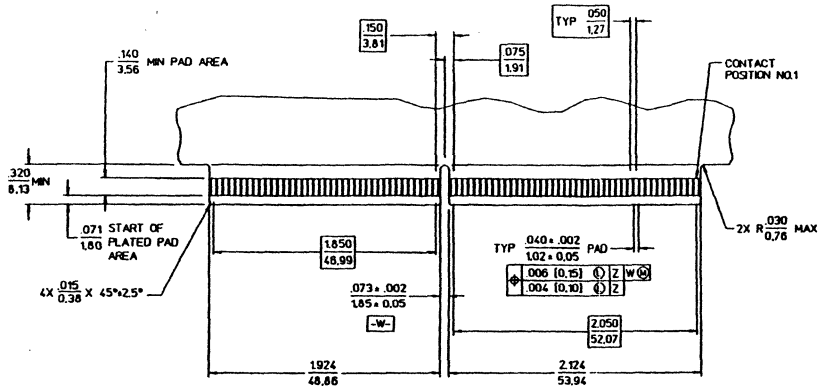
BURNDY
an FCI Company
NORWALK, CT 06850

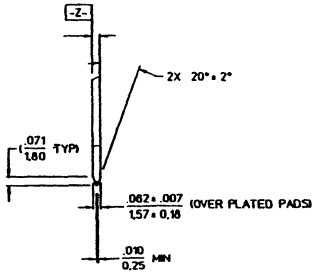
DRAWING NO BRSE94875 | REV 0

SHEET 1 OF 2

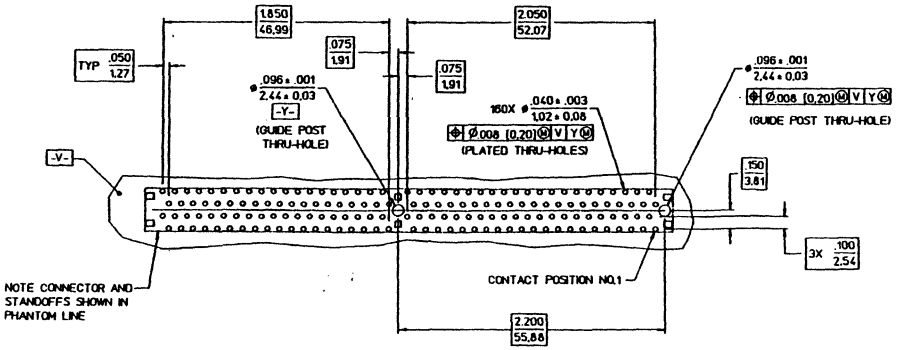
DWG RELEASED TO CENTRAL FILE 04-24-92 | CAD APPROVAL XXX XX-XX-XX

NOTES SEE SHEET 1.





MATING P.C. BOARD CONTACT PAD LAYOUT
FOR CEE2X80S-26Z14 CONNECTOR
(TYPICAL FOR BOTH SIDES).



COMPONENT SIDE

BACKPLANE LAYOUT FOR CEE2X80S-26Z14
CONNECTOR SOLDER TAILS AND GUIDE POSTS

REV	REVISION DESCRIPTION	BY	CHKD	DATE
	ALL REV. RECORDED ON SHEET 1.			

CAGE NO 09922 | DON641 | PC 822

RECOMMENDED MATING P.C. BOARD CONTACT PAD AND BACKPLANE LAYOUTS

CAT NO CEE2X80S-26Z14 | SCALE 2 : 1

DRAWN	AEW 03-20-92	APPROVALS	DSGN YIP 04-01-92
CHECKED	VCE 03-24-92		MKT BM 04-02-92
			QC JB 04-20-92

BURNDY
an FCI Company
NORWALK, CT 06856

DRAWING NO BRSE94875 | REV 0

SHEET 2 OF 2

LINEAR MEASURE: INCH mm INCH [mm]
THIRD ANGLE PROJECTION
- TOLERANCES -
UNLESS OTHERWISE SPECIFIED

NO OF DECIMAL PLACES IN INCHES	INCH [mm]
ONE PLACE	±.1 [±2.5]
TWO PLACES	±.02 [±0.5]
THREE PLACES	±.005 [±0.13]

ANGLES ±1°

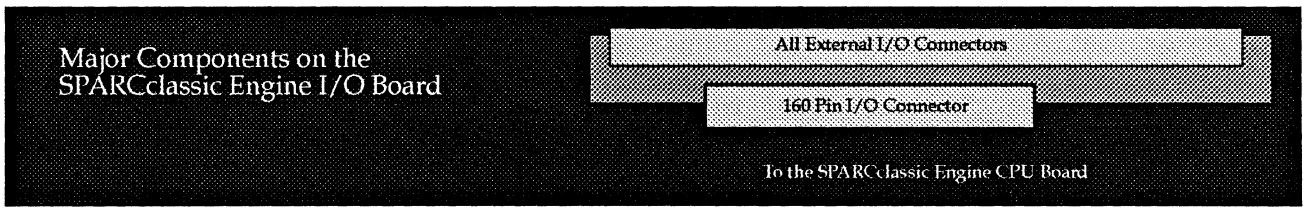
DWG RELEASED TO CENTRAL FILE 04-27-92 | CAD APPROVAL XXX XX-XX-XX

SPARCclassic Engine I/O Board

G.1 SPARCclassic Engine I/O Board Features

- External connectors
  - One female I/O connector (connection with CPU board)
  - One female SCSI 2 connector
  - One female Ethernet (Twisted-Pair) connector
  - One female Ethernet (AUI) / CHI (Monitor Port) connector
  - One female serial A/B connector
  - One female keyboard/mouse connector
  - One female parallel (printer) connector
  - One female video-out connector
  - One female headphone output connector (stereophonic)
  - One female microphone input connector (monophonic)
  - One female ISDN Network Terminal connector
  - One female ISDN Terminal Equipment connector

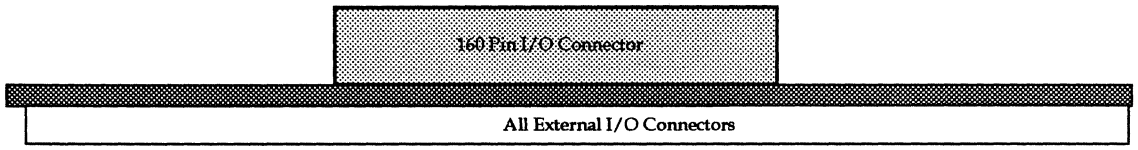
Figure G-1 Major Components on the SPARCclassic Engine I/O Board



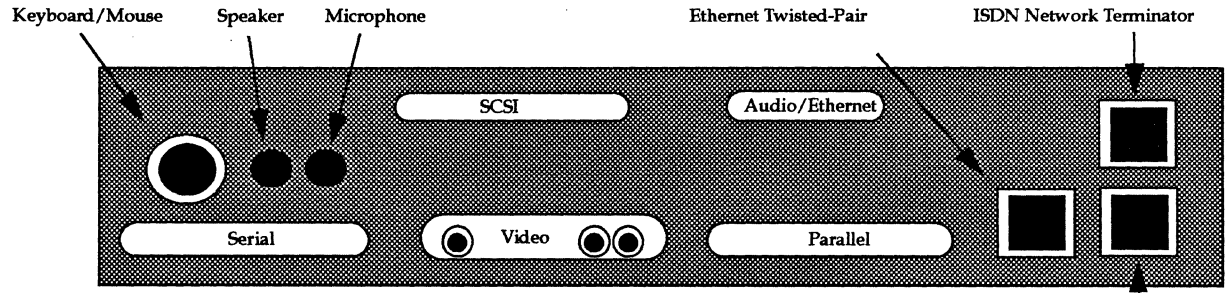
G.2 *Description of the SPARCclassic Engine I/O Board*

The SPARCclassic Engine I/O board has a 160-pin I/O female connector that connects to the SPARCclassic Engine's male edge connector (or a CPU board of your own design). The SPARCclassic Engine I/O board provides additional I/O connectors. All input/output signals pass through the 160-pin connector to SPARCclassic Engine and the various I/O connectors without modification.

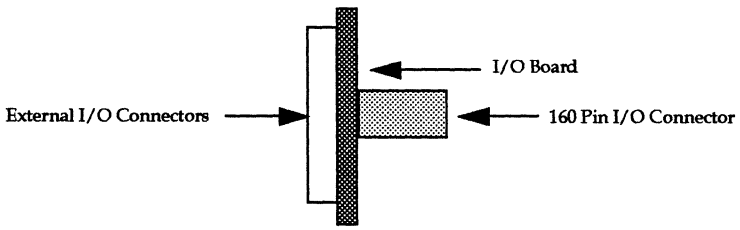
Figure G-2 Views of the SPARCclassic Engine I/O Board



TOP VIEW



FRONT VIEW



SIDE VIEW

G.2.1 160-Pin I/O Female Connector

The shielded 160-pin female connector mates with the 160-pin male edge connector of the SPARCclassic Engine board. See **Appendix E** for further specifications.

G.2.2 SCSI Connector

A 50-pin high-density connector. Term Power is fuse protected with an automatically re-setting positive temperature coefficient thermistor, so as to eliminate customer replacement of fuses. The SCSI connector has an active terminator.

G.2.3 Serial A/B Connector

Serial ports A & B share a single 25-pin D-subminiature connector. If your design requires only one port, use a direct cable and the default serial port A is utilized. If your design requires both ports, a splitter cable is required.

The connector pinout configuration allows serial port A to have a full RS-232C synchronous/asynchronous signal complement, and serial port B is wired to pins unused by serial port A, in the asynchronous mode only.

G.2.4 Parallel Port Connector

The IBM-compatible port is implemented with a 25-pin D-subminiature connector.

G.2.5 Video / Monitor Port Connector

A combined video output port and new Monitor Port signal combination implemented with a single 13W3 D-type socket housing with coax cavities.

For future compatibility, it is recommended that the Monitor Port signals be reserved for future use. However, if your design does not require a monitor, there is no restriction on alternative uses of these signals. The Sun-specific Monitor Port has been developed for future applications for keyboard control of new monitors. Signals for the Monitor Port are received through the video

connector. The mouse port transmit signals are used for the monitor port, and the mouse port receive signals are multiplexed with the signals for the monitor port. The resulting signals are forwarded to SLAVIO for processing.

G.2.6 *Keyboard/Mouse Connector*

The keyboard/mouse port is implemented with a Mini-DIN 8 connector.

G.2.7 *Loudspeaker (Stereophonic) Connector*

A standard RCA miniature-jack is used for the stereophonic loudspeakers connector.

G.2.8 *Microphone (Monophonic) Connector*

A standard RCA miniature-jack is used for the microphone connector. The pinout is non-standard. The microphone has one audio signal only, resulting in monophonic sound. The other signal is used for device power (in the Sun Microsystems configurations, the power for a powered microphone).

G.2.9 *Ethernet (AUI) / Audio (CHI) Connector*

A Ethernet AUI signals are, in this non-standard pinout, combined with audio CHI signals (in the Sun Microsystems configuration, to support an external speakerbox). The combined connector is a 26-pin Ultra-D connector. (The CHI signals are designed for a speakerbox in Sun Microsystems configurations.)

A special splitter interface cable is required st separate the signals into AUI and CHI, with the appropriate standard connectors.

G.2.10 *Twisted-Pair Ethernet Connector*

A standard RJ-45 telephone jack.

G.2.11 *ISDN Network Terminator (Line) Connector*

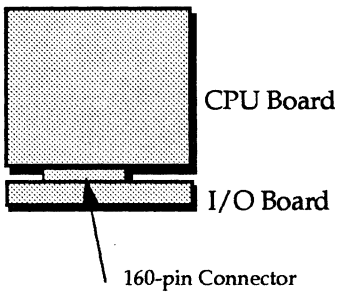
A standard RJ-45 telephone jack.

G.2.12 *ISDN Terminal Equipment (Phone) Connector*

A standard RJ-45 telephone jack.

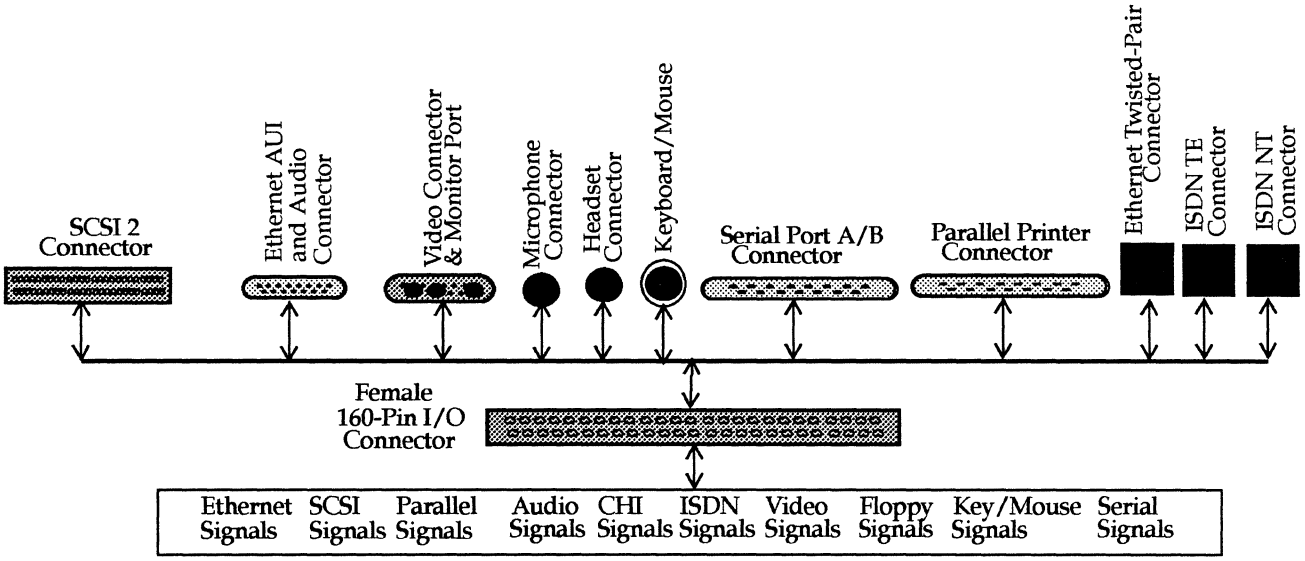
G.3 *The SPARCclassic Engine I/O Board Description.*

The SPARCclassic Engine I/O board provides additional I/O connectors.



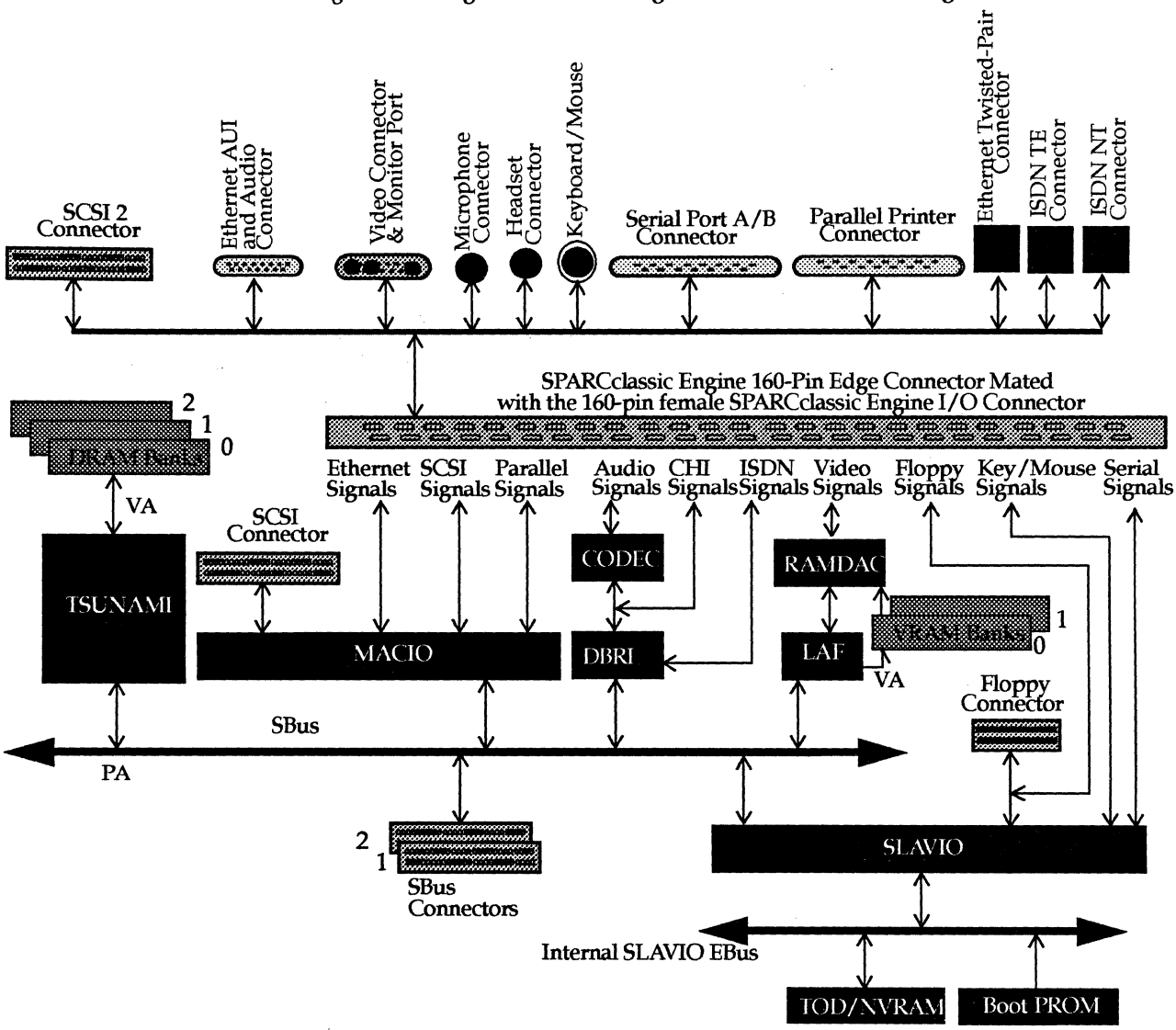
The block diagram below shows the I/O board with the various connectors:

Figure G-3 High-Level Block Level Diagram of the SPARCclassic Engine I/O Board



The SPARCclassic Engine I/O board female 160-pin I/O connector and the SPARCclassic Engine board male 160-pin edge-connector are designed to be mated. The combined CPU and I/O boards are shown together in the following block diagram:

Figure G-4 High-Level Block Diagram of the SPARCclassic Engine & I/O Boards



G.4 System Considerations

G.4.1 SPARCclassic Engine and SPARCclassic Engine I/O

The SPARCclassic Engine board and the SPARCclassic Engine I/O board are designed as a unit to create a full-function workstation. The SPARCclassic Engine board can be used alone with no I/O board. The SPARCclassic Engine can be mated with a customer-designed I/O board. The SPARCclassic Engine I/O board can be used independently with a customer-designed CPU board.

G.4.2 Other System Components

The SPARCclassic Engine I/O board, when used with SPARCclassic Engine or connected to a CPU board of your own design, allows many other devices to be connected. These devices include stereophonic speakers, stereophonic headphones, monophonic microphones, video monitors, Sun-standard keyboards, Sun-standard mice, additional SCSI devices, audio control boxes (non-MIDI), parallel printers, Ethernet and ISDN network drops.

There are many variations of equipment possible. These additional components must be purchased separately.

G.5 How to Order the SPARCclassic Engine I/O Board

Use the SunSpares Price List from Sun Microsystems to order Sun Microsystems Spares Part Number 501-2198.

G.6 SPARCclassic Engine I/O Board Specifications

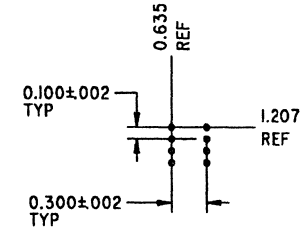
Category	Specifications
Physical Dimensions	
Long axis	230.28 mm (9.052 in.)
Short axis	36.43 mm (1.432 in.)
Connectors	
I/O (CPU connector)	1 female 160-pin shielded
SCSI Port	1 female 50-pin double-row polarized
Printer Port	1 female 25-pin double-row D-subminiature
Serial A/B Port	1 female 25-pin double-row D-subminiature
Video/Monitor Port	1 female 19-pin 13W3 D
Ethernet AUI/CHI Port	1 female 26-pin Ultra-D
ISDN NT Port	1 female 8-pin RJ-45 telephone jack
ISDN TE Port	1 female 8-pin RJ-45 telephone jack
Ethernet Twisted-Pair	1 female 8-pin RJ-45 telephone jack
Speaker (stereo) Port	1 female RCA audio miniature-jack
Microphone (mono) Port	1 female RCA audio miniature-jack
Keyboard/Mouse Port	1 female 8-pin Miniature-DIN 8

SPARCclassic Engine I/O Drawings

On the next few pages are the SPARCclassic Engine I/O board mechanical drawings. Use the drawings to determine the product size and shape.

UNRELEASED DRAWING

DO NOT MANUFACTURE. ANY CHANGES TO THIS DRAWING REQUIRES THE APPROVAL OF _____



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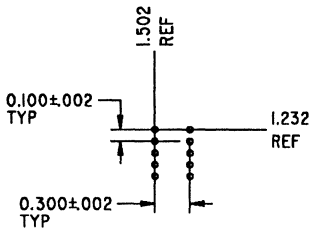

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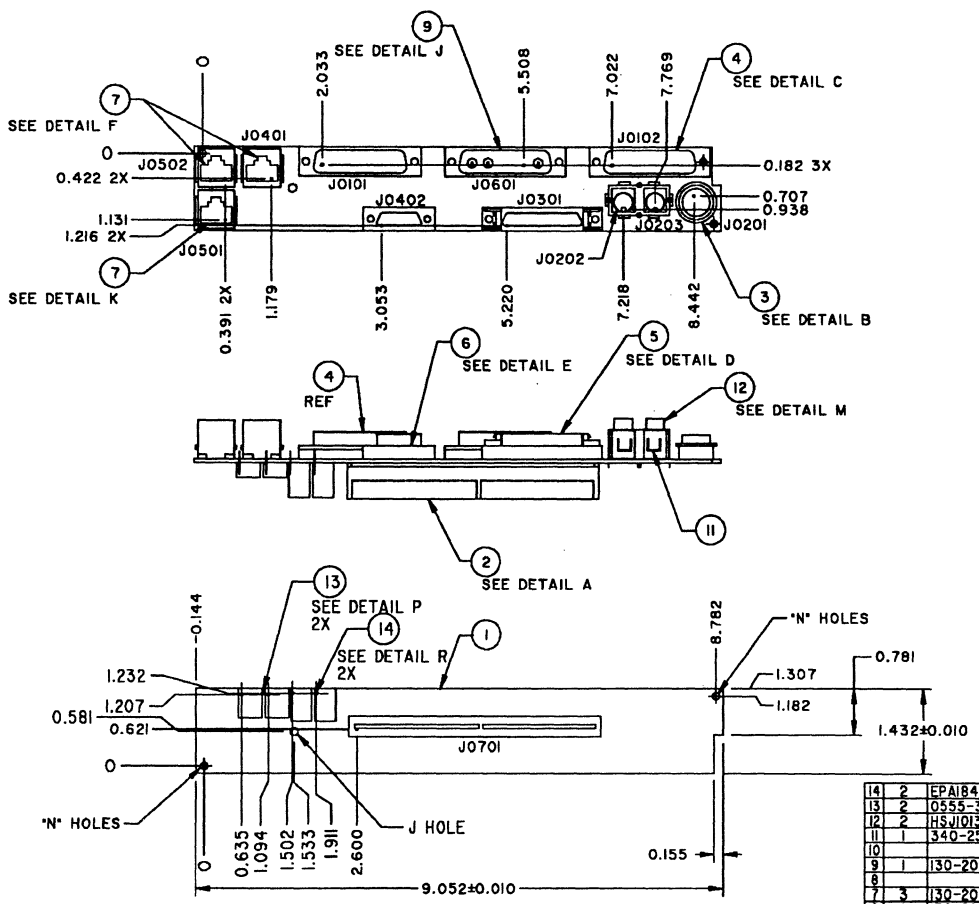

DWG. NO.	SHT	REV

REVISIONS

SUFFIX	REV.	DESCRIPTION	DATE	APPROVED
	01	INITIAL PRERELEASE	22 MAR 91	
	02	UPDATE 13W3 CONN	01 APR 91	
	03	ADD PIN DESIG. TO J0701	16 APR 91	
	04	MOVED J0301 .300, INCREASED LNG BOARD .039	25 APR 91	
	05	MOVED J0102 J0601 J0101 ADDED AUDIO JACKS J0202,J0203	06 MAY 91	
	06	MOVED J0701,REMOVED FROM DWG ITEMS 8, 10, 11	5 JUNE 91	
	07	MOVED J0701 AND CORRECTED HOLE PATTERN, ADDED NOTE 5 RE-NUMBERED PIN OUTS J0701 SWAPPED NO. J0101 AND J0102	1 JULY 91	
	08	CHG HOLE PATTERN ITEM 7 DIMENSION FROM 0.300 TO 0.153. ADDED LANDING FOR EMI CAN ITEM 12	11 JUL 91	
	09	CORRECTED QUANTITY OF ITEM 3	16 AUG 91	
	10	DET E: DELETED 2 J HOLES .272 WAS .240, ADDED .024 9.052..144 WAS 9.072. .164	06 NOV 91	
	11	ADD ISDN CHOKES & THRU HOLE	30 JAN 92	

HOLE LEGEND

SYM	DESCRIPTION	QTY
A	Ø0.040 ±0.003 PTH	160
B	Ø0.096 ±0.001 NON-PTH	2
C	Ø0.035 ±0.003 PTH	68
D	Ø0.071 ±0.003 PTH	2
E	Ø0.120 ±0.002 PTH	4
F	Ø0.041 ±0.002 PTH	69
G	Ø0.029-Ø0.039 PTH	50
H	Ø0.109 ±0.002 NON-PTH	2
I	Ø0.031 ±0.002 PTH	26
J	Ø0.135 ±0.002 NON-PTH	1
K	Ø0.062 ±0.002 PTH	9
L	Ø0.128 ±0.003 NON-PTH	6
M	Ø0.062 ±0.002 NON-PTH	1
N	Ø0.125 ±0.003 NON-PTH	2
O	Ø0.125 ±0.003 PTH	2
P	Ø0.075 ±0.002 PTH	2
Q	Ø0.136 ±0.002 PTH	2
R	Ø0.078 ±0.002 PTH	10

NOTES:

1. ALL DIMENSIONS ARE IN INCHES.
2. MATERIAL: EPOXY FIBERGLASS FR-4 UL FLAME RATING 94V0, 0.062 THK.
3. ALL DIMENSIONS LOCATING CONNECTORS ARE TO PIN 1.
4. PCB SHALL BEAR UR APPROVAL, VENDOR DATE CODE AND COUNTRY OF ORIGIN.
5. EXTERNAL LAYERS TO HAVE GROUND ETCH ONLY (SOLDER MASK PERMISSABLE). INTERNAL LAYER SIGNAL RUNS TO BE 0.060 MINIMUM FROM EDGE.
6. AREA TO BE FREE OF VIA'S AND COMPONENTS. (NEARSIDE)

ITEM	QTY	PART NO.	DESCRIPTION
14	2	EPAI846	ISDN CHOKE PCA ELECTRONICS
13	2	0555-3536-00	ISDN COMMON MODE CHOKE BEL FUSE
12	2	HSJ1013-01-120	MINIATURE JACK, HOSIDEN
11	1	340-2583-01	SHIELD, EMI, AUDIO, SUNERGY
10			
9	1	130-2011-01	CONN, RECEPT, VERTICAL, 13W3, 236
8			
7	3	130-2007-01	MOD JACK, 8 POS, SHIELDED, 236 HG
6	1	130-2010-01	CONN, ULTRA-D, VERTICAL, RECEPT
5	1	130-2009-01	CONN, 50P, SCSI 2, VERTICAL, 236
4	2	AMP# 747708	AMP, RECEPT, VERTICAL, 25 POS
3	1	130-2008-01	MINI DIN, 8 POS, VERTICAL SHIELD
2	1	130-1863-01	CONN, EDGE CARD, 160 POS
1	N/A	XXX-XXXX-XX	PCB, I/O, CURLY, SUNERGY

PART LIST

ENGLISH
THIRD ANGLE PROJECTION

APPROVALS	DATE
DRAWN BOBA	22 MAR 91
CHECKED	
ISSUED BOBA	6 JUNE 91
RELEASED	

MATERIAL 2
FINISH

DO NOT SCALE DRAWING

sun

OUTLINE DWG, I/O, CURLY, SUNERGY

SIZE D DWG NO. 270-1887-50 REV. 12
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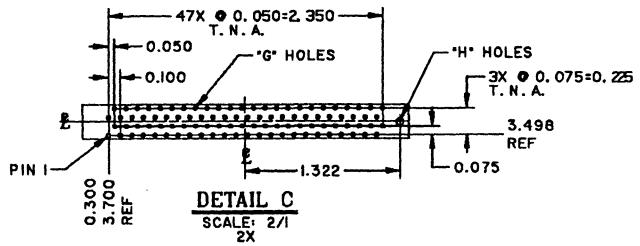

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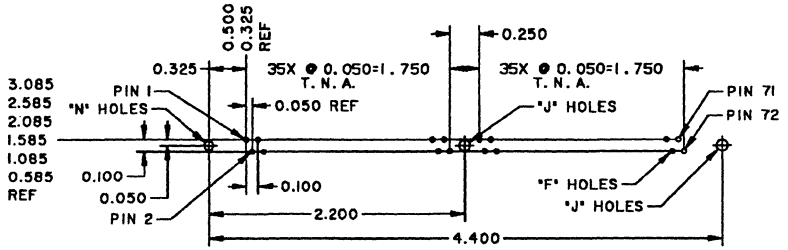

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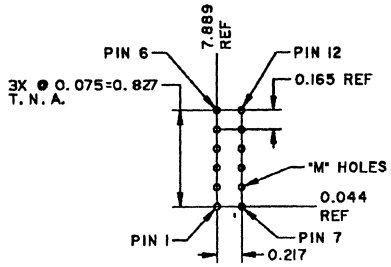

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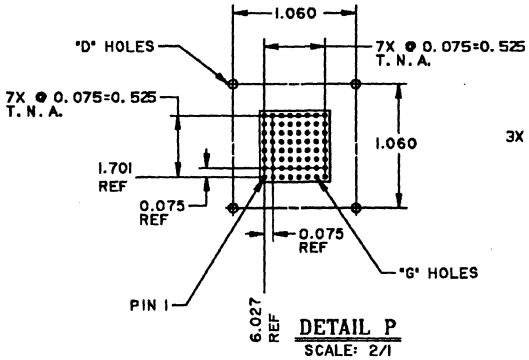

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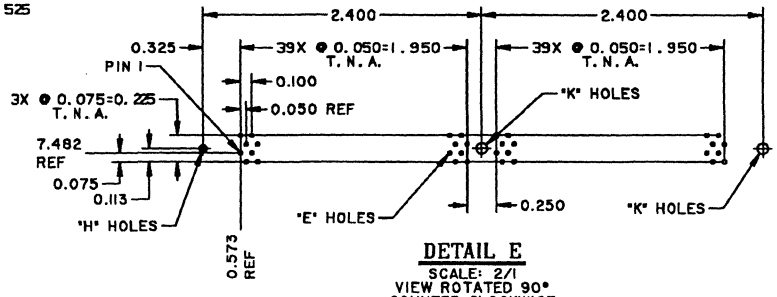

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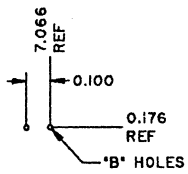
FOR CLARITY



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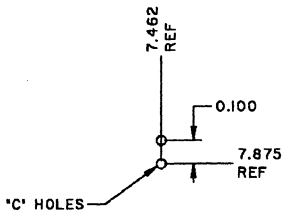

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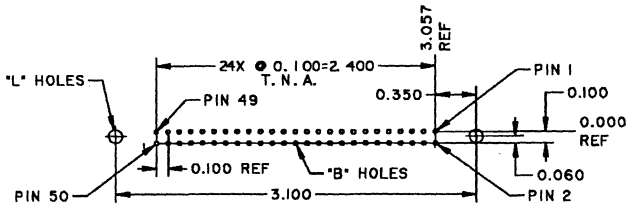

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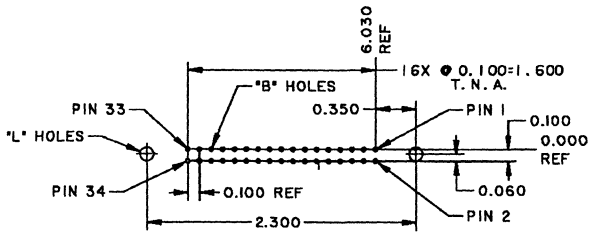

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sun

SIZE	DWG NO.	REV.
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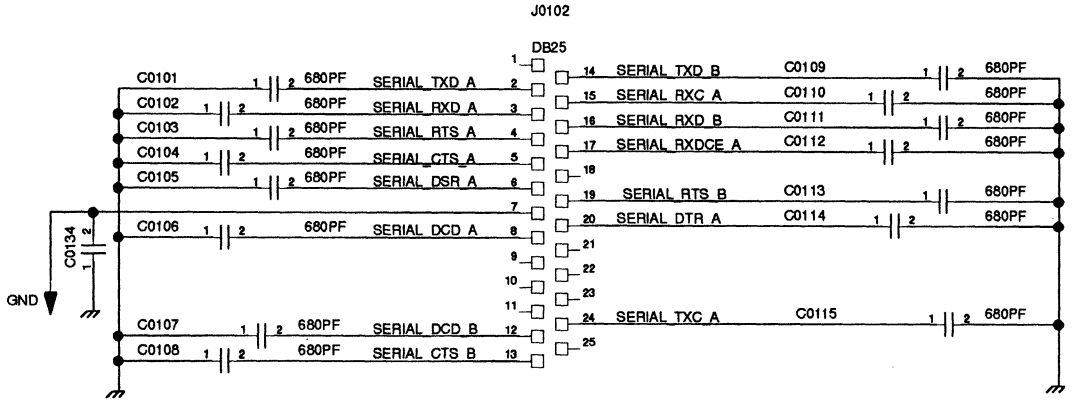
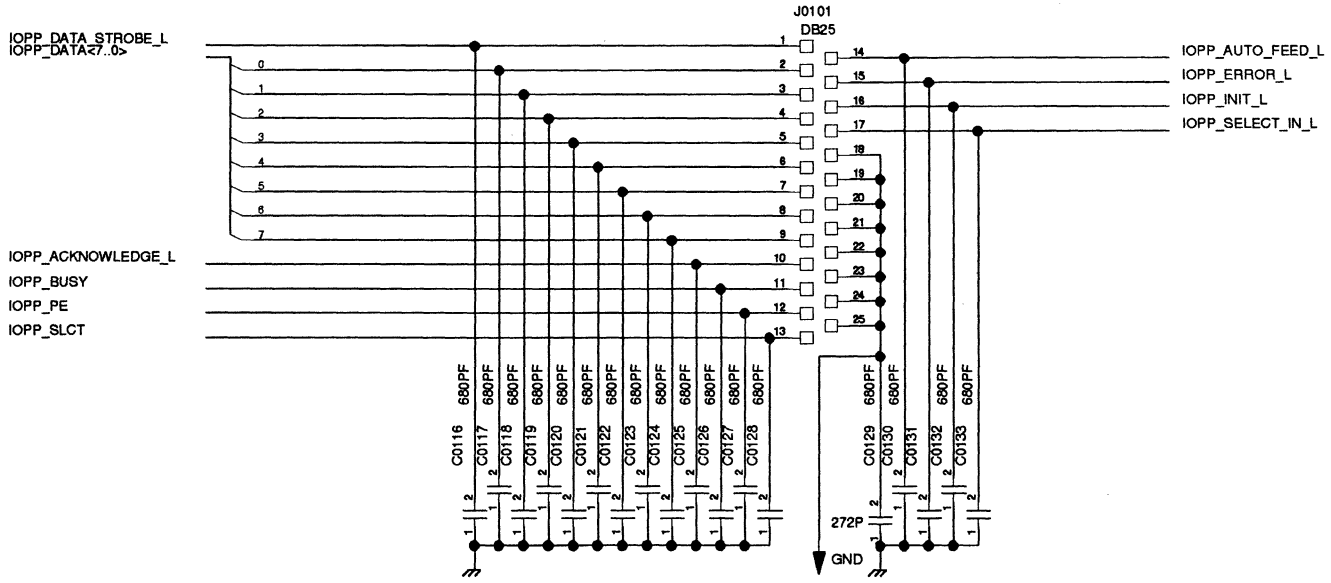
SPARCclassic Engine I/O Schematics

On the next few pages are the SPARCclassic Engine I/O board schematics.

Serial Ports



Parallel Port



sun microsystems

DRAWING

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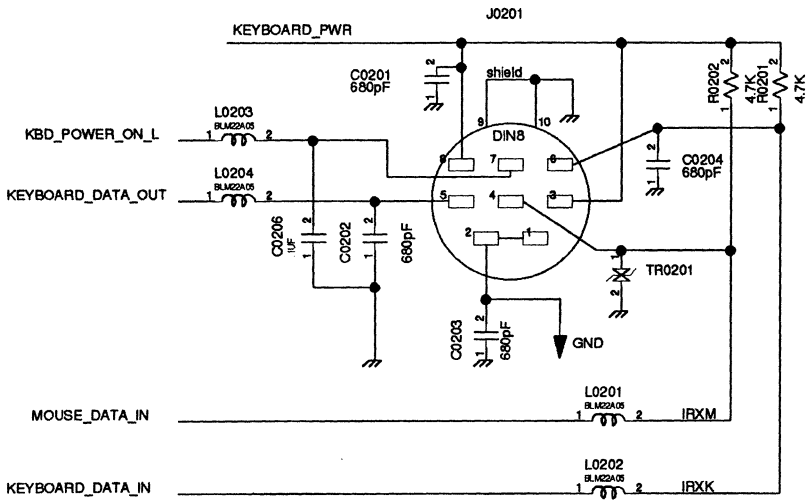
SHEET: 1 OF
ENGINEER:

SUNPARTNR: 502-1887-01

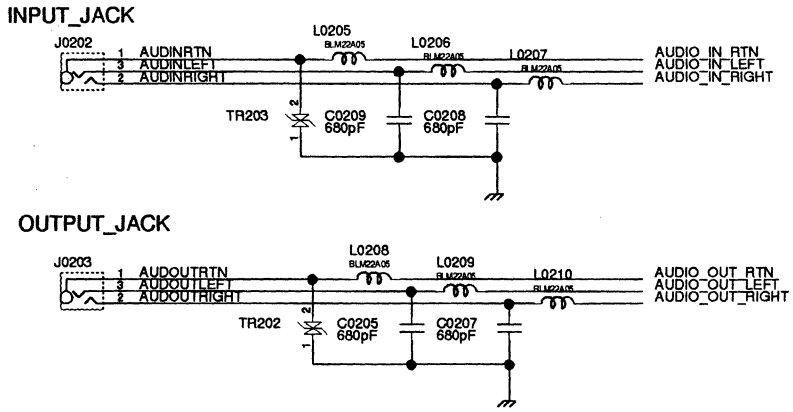
REV: P2

DATE: Thu Jan 9 10:16:43 1992

Mouse/Keyboard Connectors



AUDIO CONNECTORS



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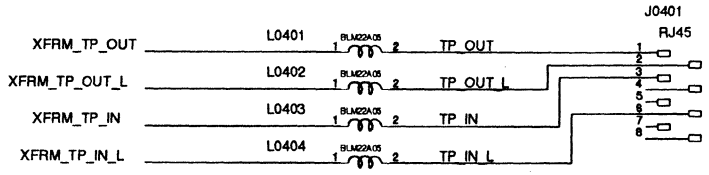
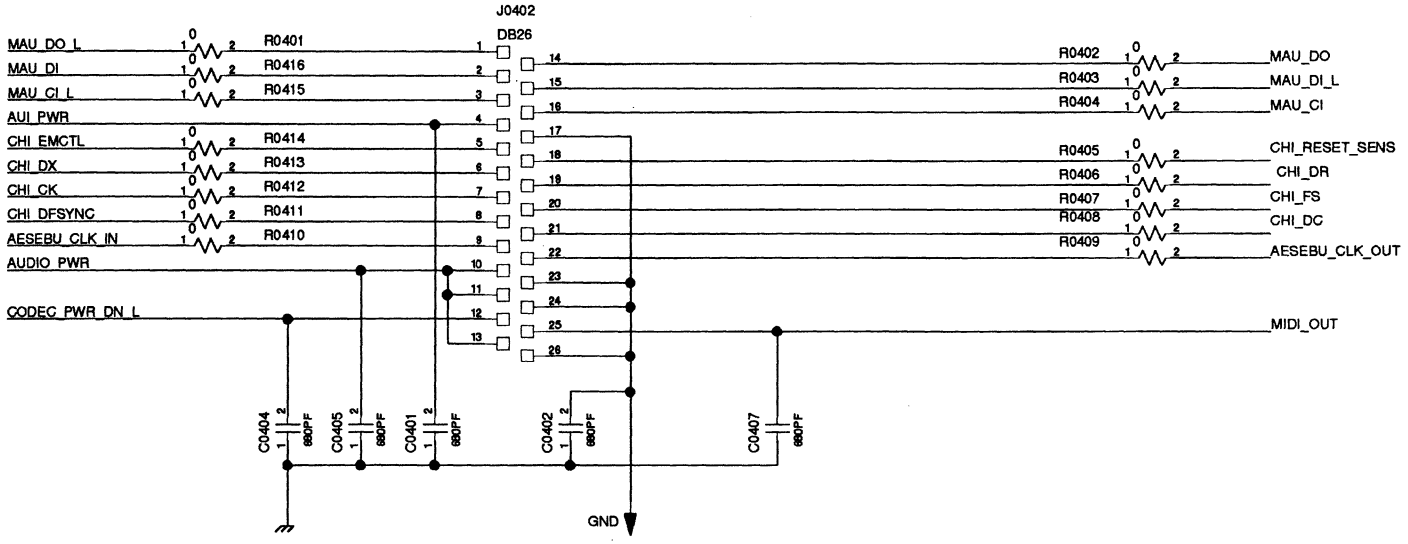
TWISTED PAIR ETHERNET



CHI/AUI ETHERNET



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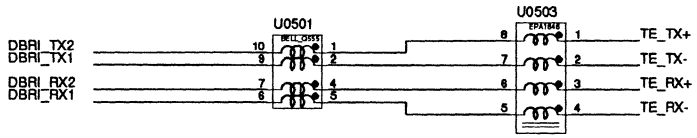

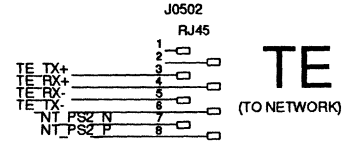

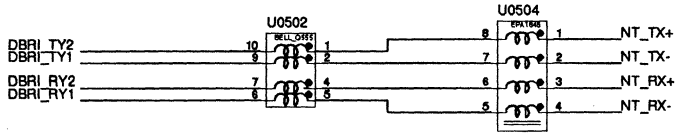

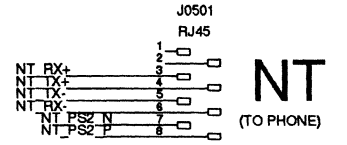

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SHEET: 5 OF
ENGINEER:

SUNPARTNR: 502-1887-01
DATE: Thu Jan 16 16:54:59 1992

REV: P2

TDK ZJSC-R10-470

U0601

EMI_BLUE — 1 — 3 — BLUE

2

VIDEO_GND

TDK ZJSC-R10-470

U0602

EMI_GREEN/MONO — 1 — 3 — GREEN/MONO

2

VIDEO_GND

TDK ZJSC-R10-470

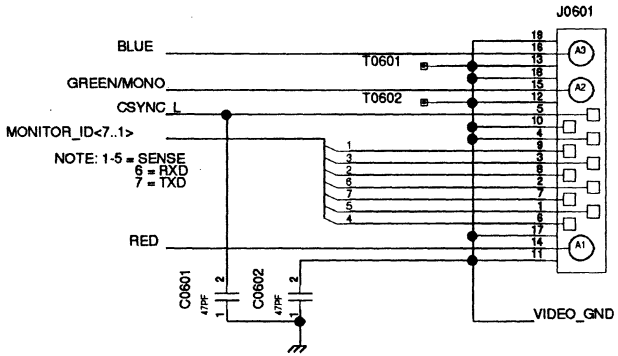
U0603

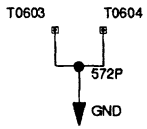
EMI_RED — 1 — 3 — RED

2

VIDEO_GND

VIDEO Connector





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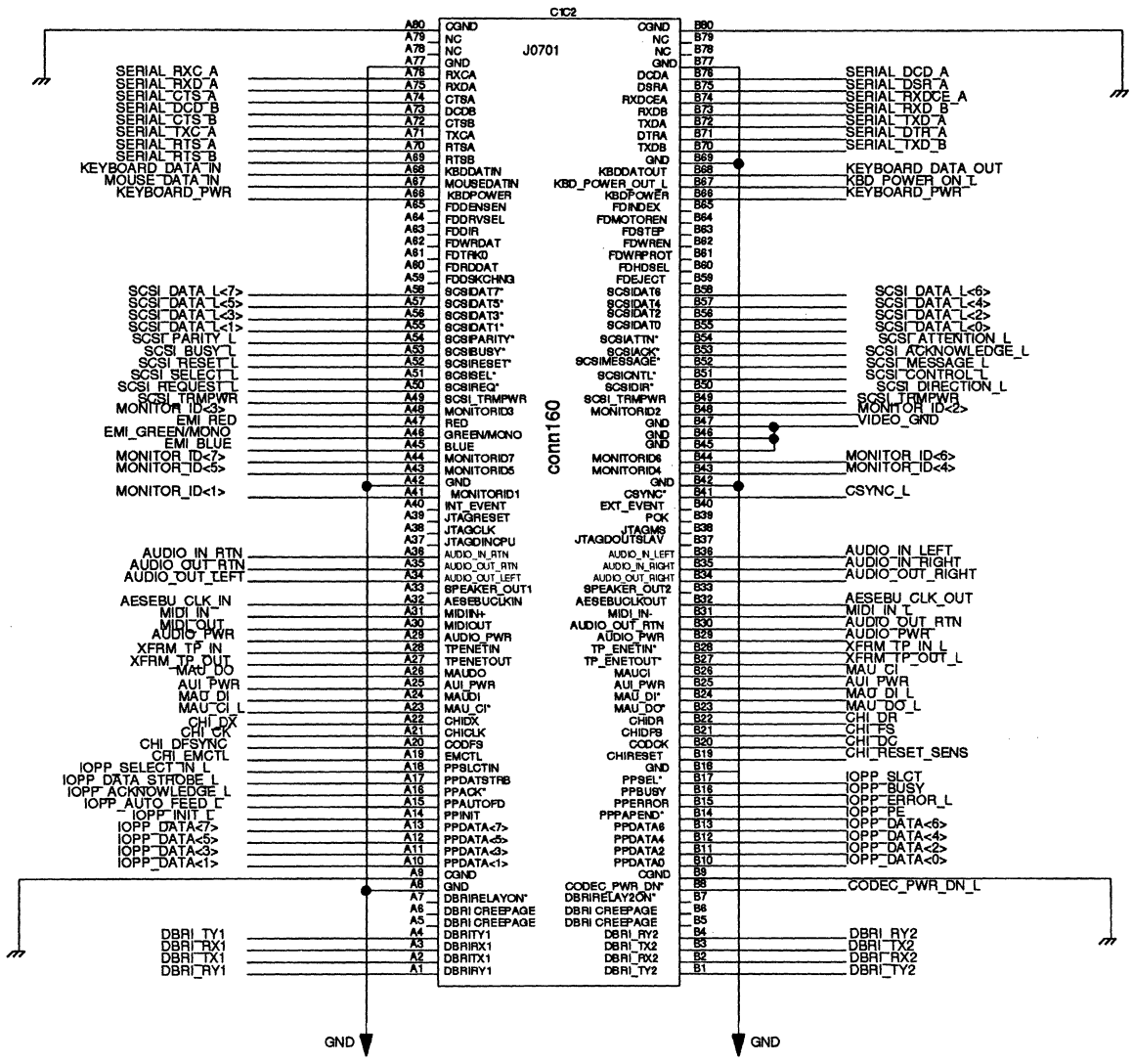

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SUNPARTNR: 502-1887-01

DATE: Fri Jan 24 17:46:20 1992

REV: P2

SPARCclassic Engine I/O Pinouts

J.1 160-Pin Female I/O Connector Pinout List

Reference Identifier: J0701

Connector Type: 160-pin shielded special connector

(Burndy #CEE2X80S-26Z14)

I/O Standard Pinouts	Pin #	SPARCclassic Engine I/O Signals
DBRI_RY1	A1	DBRI_RY1
DBRI_TX1	A2	DBRI_TX1
DBRI_RX1	A3	DBRI_RX1
DBRI_TY1	A4	DBRI_TY1
DBRI creepage	A5	
DBRI creepage	A6	
DBRI creepage	A7	
GND	A8	GND
CGND	A9	Chassis Ground
PPDATA<1>	A10	IOPP_DATA<1>
PPDATA<3>	A11	IOPP_DATA<3>
PPDATA<5>	A12	IOPP_DATA<5>
PPDATA<7>	A13	IOPP_DATA<7>
PPINIT	A14	IOPP_INIT_L
PPAUTOFD	A15	IOPP_AUTO_FEED_L
PPACK*	A16	IOPP_ACKNOWLEDGE_L
PPDATASTRB	A17	IOPP_DATA_STROBE_L

PPSLCTIN	A18	IOPP_SELECT_IN_L
EMCTL	A19	CHI_EMCTL
CODFS	A20	CHI_DFSYNC
CHICLK	A21	CHI_CK
CHIDX	A22	CHI_DX
MAU_CI*	A23	MAU_CI_1
MAUDI	A24	MAU_DI
AUI_PWR	A25	AUI_PWR
MAUDO	A26	MAU_DO
TPENETOUT	A27	XFRM_TP_OUT
TPENETIN	A28	XFRM_TP_IN
AUDIO_PWR	A29	AUDIO_PWR
MIDIOUT	A30	MIDI_OUT
MIDIIN+	A31	MIDI_IN
AESEBUCLKIN	A32	AESEBU_CLK_IN
SPEAKER_OUT1	A33	
AUDIO_OUT_LEFT	A34	AUDIO_OUT_LEFT
AUDIO_OUT_RTN	A35	AUDIO_OUT_RTN
AUDIO_IN_RTN	A36	AUDIO_IN_RTN
JDTAGDINCPU	A37	JTAG_D_IN
JTAGCLK	A38	JTAG_CLK
JTAGRESET	A39	JTAG_RESET
INT_EVENT	A40	
MONITORID1	A41	MONITOR_ID<1>
GND	A42	GND
MONITORID5	A43	MONITOR_ID<5>
MONITORID7	A44	MONITOR_ID<7>
BLUE	A45	EMI_BLUE
GREENMONO	A46	EMI_GREEN/MONO
RED	A47	EMI_RED
MONITORID3	A48	MONTITOR_ID<3>
SCSI_TRMPWR	A49	SCSI_TRMPWR
SCSIREQ*	A50	SCSI_REQUEST_L
SCSISEL*	A51	SCSI_SELECT_L
SCSIRESET*	A52	SCSI_RESET_L
SCSIBUSY*	A53	SCSI_BUSY_L
SCSIPARITY*	A54	SCSI_PARITY_L
SCSIDAT1*	A55	SCSI_DATA_L<1>
SCSIDAT3*	A56	SCSI_DATA_L<3>
SCSIDAT5*	A57	SCSI_DATA_L<5>

SCSIDAT7*	A58	SCSI_DATA_L<7>
FFDSKCHNG	A59	
FDRDDAT	A60	
FDTRK0	A61	
FDWRDAT	A62	
FDDIR	A63	
FDDRVSEL	A64	
FDDENSEN	A65	
KBDPOWER	A66	KEYBOARD_PWR
MOUSEDATIN	A67	MOUSE_DATA_IN
KBDATIN	A68	KEYBOARD_DATA_IN
RTSB	A69	SERIAL_RTS_B
RTSA	A70	SERIAL_RTS_A
TXCA	A71	SERIAL_TXC_A
CTSB	A72	SERIAL_CTS_B
DCDB	A73	SERIAL_DCD_B
CTSA	A74	SERIAL_CTS_A
RXDA	A75	SERIAL_RXD_A
RXCA	A76	SERIAL_RXC_A
GND	A77	GND
TXCB	A78	SERIAL_TXC_B
RXCB	A79	SERIAL_RXC_B
CGND	A80	Chassis Ground
DBRI_TY2	B1	DBRI_TY2
DBRI_RX2	B2	DBRI_RX2
DBRI_TX2	B3	DBRI_TX2
DBRI_RY2	B4	DBRI_RY2
DBRI creepage	B5	
DBRI creepage	B6	
DBRI creepage	B7	
CODEC_PWR_DN*	B8	CODEC_PWR_DN_L
CGND	B9	Chassis Ground
PPDATA<0>	B10	IOPP_DATA<0>
PPDATA<2>	B11	IOPP_DATA<2>
PPDATA<4>	B12	IOPP_DATA<4>
PPDATA<6>	B13	IOPP_DATA<6>
PPPAPEND*	B14	IOPP_PE
PPERROR	B15	IOPP_ERROR_L
PPBUSY	B16	IOPP_BUSY
PPSEL*	B17	IOPP_SLCT

GND	B18	GND
CHIRESET	B19	CHI_RESET_SENS
CODCK	B20	CHI_DC
CHIDFS	B21	CHI_FS
CHIDR	B22	CHI_DR
MAU_DO*	B23	MAU_DO_L
MAU_DI*	B24	MAU_DI_L
AUI_PWR	B25	AUI_PWR
MAUCI	B26	MAU_CI
TP_ENETOUT*	B27	XFRM_TP_OUT_1
TP_ENETIN*	B28	XFRM_TP_IN_L
AUDIO_PWR	B29	AUDIO_PWR
AUDIO_OUT_RTN	B30	AUDIO_OUT_RTN
MIDI_IN-	B31	MIDI_IN_L
AESEBUCLKOUT	B32	AESEBU_CLK_OUT
SPEAKER_OUT2	B33	
AUDIO_OUT_RIGHT	B34	AUDIO_OUT_RIGHT
AUDIO_IN_RIGHT	B35	AUDIO_IN_RIGHT
AUDIO_IN_LEFT	B36	AUDIO_IN_LEFT
JDTAGDOUTSLAV	B37	JTAG_DOUT
JTAGMS	B38	JTAG_MS
POK	B39	POK
EXT_EVENT	B40	
CSYNC*	B41	CSYNC_L
GND	B42	GND
MONITORID4	B43	MONITOR_ID<4>
MONITORID6	B44	MONITOR_ID<6>
GND	B45	GND (Video)
GND	B46	GND (Video)
GND	B47	GND (Video)
MONITORID2	B48	MONTITOR_ID<2>
SCSI_TRMPWR	B49	SCSI_TRMPWR
SCSIDIR*	B50	SCSI_DIRECTION_L
SCSICNTL*	B51	SCSI_CONTROL_L
SCSIMESSAGE*	B52	SCSI_MESSAGE_L
SCSIIACK*	B53	SCSI_ACKNOWLEDGE_L
SCSIATTN*	B54	SCSI_ATTENTION_L
SCSIDAT0*	B55	SCSI_DATA_L<0>
SCSIDAT2*	B56	SCSI_DATA_L<2>
SCSIDAT4*	B57	SCSI_DATA_L<4>

SCSIDAT6*	B58	SCSI_DATA_L<6>
FDEJECT	B59	
FDHDSEL	B60	
FDWRPROT	B61	
FDWWREN	B62	
FDSTEP	B63	
FDMOTOREN	B64	
FDINDEX	B65	
KBDPOWER	B66	KEYBOARD_PWR
KBD_POWER_OUT_L	B67	KBD_POWER_OUT_L
KBDDATOUT	B68	KEYBOARD_DATA_OUT
GND	B69	GND
TXDB	B70	SERIAL_TXD_B
DTRA	B71	SERIAL_DTR_A
TXDA	B72	SERIAL_TXD_A
RXDB	B73	SERIAL_RDX_B
RXDCEA	B74	SERIAL_RDDCE_A
DSRA	B75	SERIAL_DSR_A
DCDA	B76	SERIAL_DCD_A
GND	B77	GND
DTRB	B78	SERIAL_DTR_B
NC	B79	Not Connected
CGND	B80	Chassis Ground

J.2 *Parallel Port Connector Pinout List*

Reference Identifier: J0101

Connector Type: A female 25-pin double-row D sub-miniature (DB-25)

Signal	Pin #	Comments
IOPP_DATA_STROBE_L	1	
IOPP_DATA<0>	2	
IOPP_DATA<1>	3	
IOPP_DATA<2>	4	
IOPP_DATA<3>	5	
IOPP_DATA<4>	6	
IOPP_DATA<5>	7	
IOPP_DATA<6>	8	
IOPP_DATA<7>	9	
IOPP_ACKNOWLEDGE_L	10	
IOPP_BUSY	11	
IOPP_PE	12	
IOPP_SLCT	13	
IOPP_AUTO_FEED_L	14	
IOPP_ERROR_L	15	
IOPP_INIT_L	16	
IOPP_SELECT_IN_L	17	
GND	18	
GND	19	
GND	20	
GND	21	
GND	22	
GND	23	
GND	24	
GND	25	

J.3 *Video Output & Monitor Port Connector Pinout List*

Reference Identifier: J0601

Connector Type: a female 19-pin D13W3 connector

Comments	Pin #	Signal
TRANSMIT	1	MONITOR_ID<5>
GND	2	MONITOR_ID<6>
SENSE<3>	3	MONITOR_ID<3>
	4	VIDEO_GND
	5	CSYNC_L
GND	6	MONITOR_ID<4>
RECEIVE	7	MONITOR_ID<7>
SENSE<2>	8	MONITOR_ID<2>
SENSE<1>	9	MONITOR_ID<1>
	10	VIDEO_GND
	11	RED
	12	VIDEO_GND
	13	VIDEO_GND
	14	VIDEO_GND
	15	GREEN/MONO
	16	BLUE
	17	VIDEO_GND
	18	VIDEO_GND
	19	VIDEO_GND

J.4 SCSI Connector Pinout List

Reference Identifier: J0301

Connector Type: A female 50-pin double-row polarized (CONN50)

Signal	Pin #	Comments
GND	1	Ground
GND	2	Ground
GND	3	Ground
GND	4	Ground
GND	5	Ground
GND	6	Ground
GND	7	Ground
GND	8	Ground
GND	9	Ground
GND	10	Ground
GND	11	Ground
Reserved	12	Reserved
NC	13	No Connection
Reserved	14	Reserved
GND	15	Ground
GND	16	Ground
GND	17	Ground
GND	18	Ground
GND	19	Ground
GND	20	Ground
GND	21	Ground
GND	22	Ground
GND	23	Ground
GND	24	Ground
GND	25	Ground
SD0-	26	SCSI Data0-
SD1-	27	SCSI Data1-
SD2-	28	SCSI Data2-
SD3-	29	SCSI Data3-
SD4-	30	SCSI Data4-
SD5-	31	SCSI Data5-
SD6-	32	SCSI Data6-

SD7-	33	SCSI Data7-
SDP-	34	SCSI Parity-
GND	35	Ground
GND	36	Ground
Reserved	37	Reserved
TRMPWR	38	Terminator Power (~5 Volts DC, Protected, 3 Amps)
Reserved	39	Reserved
GND	40	Ground
ATN-	41	Attention-
GND	42	Ground
BSY-	43	Busy-
ACK-	44	Acknowledge-
RST-	45	Reset-
MSG-	46	Message-
SEL-	47	Select-
CD-	48	Command/Data-
REQ-	49	Request-
IO-	50	Input/Output Direction-

Pin 38 is overcurrent-protected through a diode.

J.5 Keyboard/Mouse Connector Pinout List

Reference Identifier: J0201

Connector Type: A female 8-pin miniature (DIN-8)

Pin #	Description
1	Not Connected
2	Ground
3	Keyboard Power (+5 VDC*)
4	Mouse In
5	Keyboard Out
6	Keyboard In
7	Ground**
8	Keyboard Power (+5 VDC*)

*+5V is overcurrent-protected.
** May be jumpered to MouseOutput

J.6 Ethernet Twisted-Pair (TP) Connector Pinout List

Reference Identifier: J0401

Connector Type: A female 8-pin RJ-45 telephone jack

Signal	Pin #	Comments
XFRM_TP_OUT	1	TP_OUT
XFRM_TP_OUT_L	2	TP_OUT_L
XFRM_TP_IN	3	TP_IN
NC	4	Not Connected
NC	5	Not Connected
XFRM_TP_IN_L	6	TP_IN_L
NC	7	Not Connected
NC	8	Not Connected

J.7 Serial Ports A & B Connector Pinout List

Reference Identifier: J0102

Connector Type: A female 25-pin double-row D sub-miniature (DB-25)

Signal	Pin #	Comments
NC	1	Not Connected
SERIAL_TXD_A	2	
SERIAL_RXD_A	3	
SERIAL_RTS_A	4	
SERIAL_CTS_A	5	
SERIAL_DSR_A	6	
GRD	7	Ground
SERIAL_DCD_A	8	
NC	9	Not Connected
NC	10	Not Connected
SERIAL_DTR_B	11	
SERIAL_DCD_B	12	
SERIAL_CTS_B	13	
SERIAL_TXD_B	14	
SERIAL_RXC_A	15	
SERIAL_RXD_B	16	
SERIAL_RXDCE_A	17	
SERIAL_RXC_B	18	
SERIAL_RTS_B	19	
SERIAL_DTR_A	20	
NC	21	Not Connected
NC	22	Not Connected
NC	23	Not Connected
SERIAL_TXC_A	24	
SERIAL_TXC_B	25	

J.8 ISDN Terminal Equipment (TE)

Reference Identifier: J0701

Connector Type: A female 8-pin RJ-45 telephone jack

Signal	Pin #	Comments
Connected to NT Pin 1	1	
Connected to NT Pin 1	2	
TE_TX*	3	
TE_RX*	4	
TE_RX-	5	
TE_TX-	6	
NT_PS2_N	7	
NT_PS2_P	8	

J.9 ISDN Network Terminator (NT)

Reference Identifier: J0701

Connector Type: A female 8-pin RJ-45 telephone jack

Signal	Pin #	Comments
Connected to TE Pin 1	1	
Connected to TE Pin 1	2	
NT_TX*	3	
NT_RX*	4	
NT_RX-	5	
NT_TX-	6	
NT_PS2_N	7	
NT_PS2_P	8	

J.10 Ethernet (AUI) & Audio (CHI) Connector Pinout List

Reference Identifier: J0402

Connector Type: A female 26-pin Ultra-D (DB26)

Signal	Pin #	Comments
MAU_DO_L	1	
MAU_DI	2	
MAU_CI_L	3	
AUI_PWR	4	
CHI_EMCTL	5	
CHI_DX	6	
CHI_CK	7	
CHI_DFSYNC	8	
AESEBU_CLK_IN	9	
AUDIO_PWR	10	
GND	11	Ground
CODEC_PWR_DN_L	12	
GND	13	
MAU_DO	14	
MAU_DI_L	15	
MAU_CI	16	
GND	17	Ground
CHI_RESET_SENS	18	
CHI_DR	19	
CHI_FS	20	
CHI_DC	21	
AESEBU_CLK_OUT	22	
GND	23	Ground
GND	24	Ground
MIDI_OUT	25	Reserved for Future Use
GND	26	Ground

J.11 Microphone In Connector Pinout List

Reference Identifier: J0202

Connector Type: A female RCA audio miniature-jack

Signal	Pin #	Comments
AUDIOINRTN	1	
AUDIOINLEFT	2	
AUDIOINRIGHT	3	

J.12 Headphone Out Connector Pinout List

Reference Identifier: J0203

Connector Type: A female RCA audio miniature-jack

Signal	Pin #	Comments
AUDIOOUTRTN	1	
AUDIOOUTLEFT	2	
AUDIOOUTRIGHT	3	